Thurman UMA Schematics Document

uFCPGA Mobile Merom

Intel Crestline-GM + ICH8M

2007-04-23

REV : SC (DELL:X02)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Thurman UMA		
Size: A3	Document Number: COVER PAGE	Rev: SC
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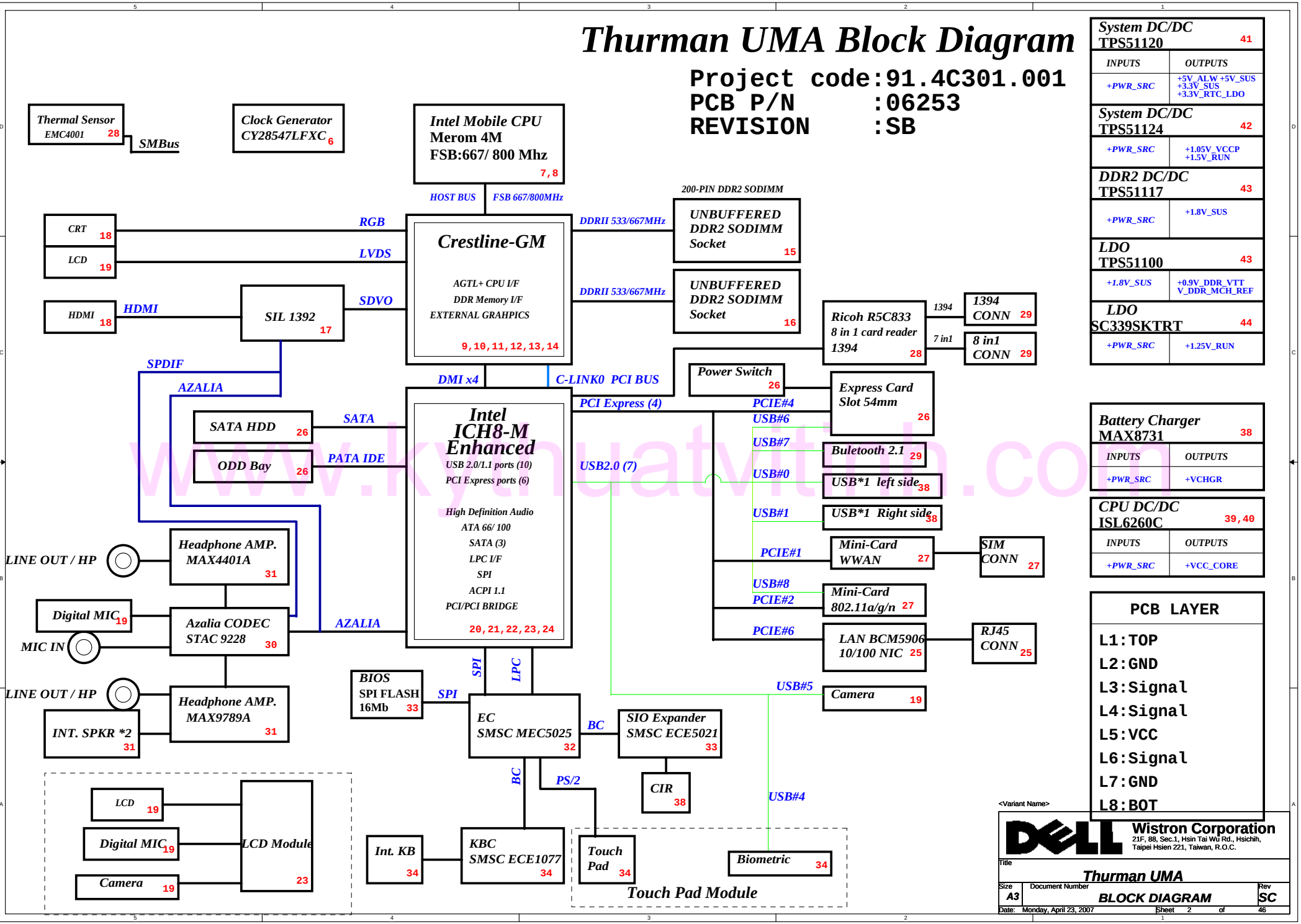
Thurman UMA Block Diagram

Project code:91.4C301.001
PCB P/N :06253
REVISION :SB



System DC/DC TPS51120 41	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO

System DC/DC TPS51124 42	
+PWR_SRC	+1.05V_VCCP +1.5V_RUN

DDR2 DC/DC TPS51117 43	
+PWR_SRC	+1.8V_SUS

LDO TPS51100 43	
+1.8V_SUS	+0.9V_DDR_VTT V_DDR_MCH_REF

LDO SC339SKTRT 44	
+PWR_SRC	+1.25V_RUN

Battery Charger MAX8731 38	
INPUTS	OUTPUTS
+PWR_SRC	+VCHGR

CPU DC/DC ISL6260C 39,40	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

PCB LAYER

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

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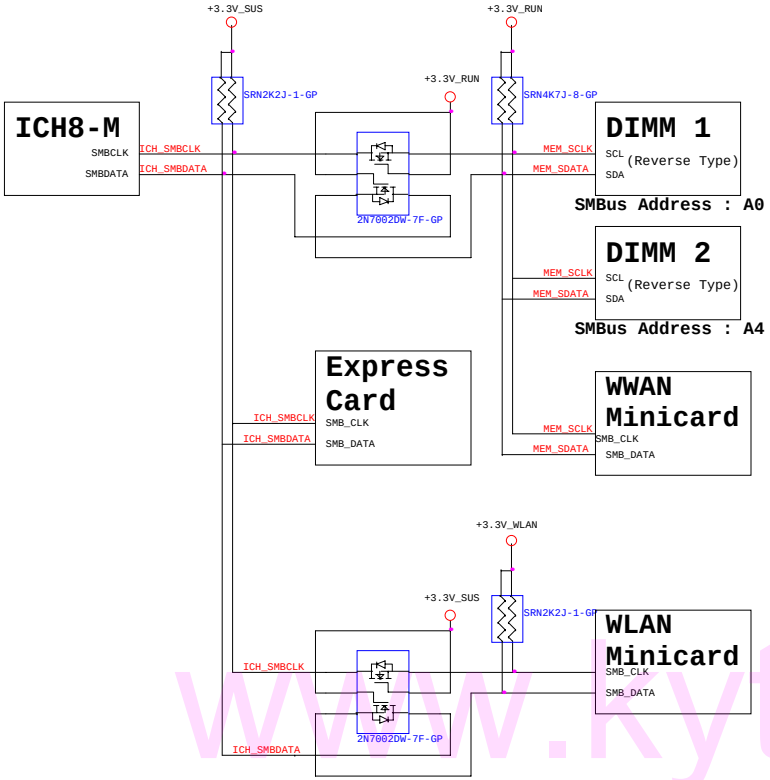
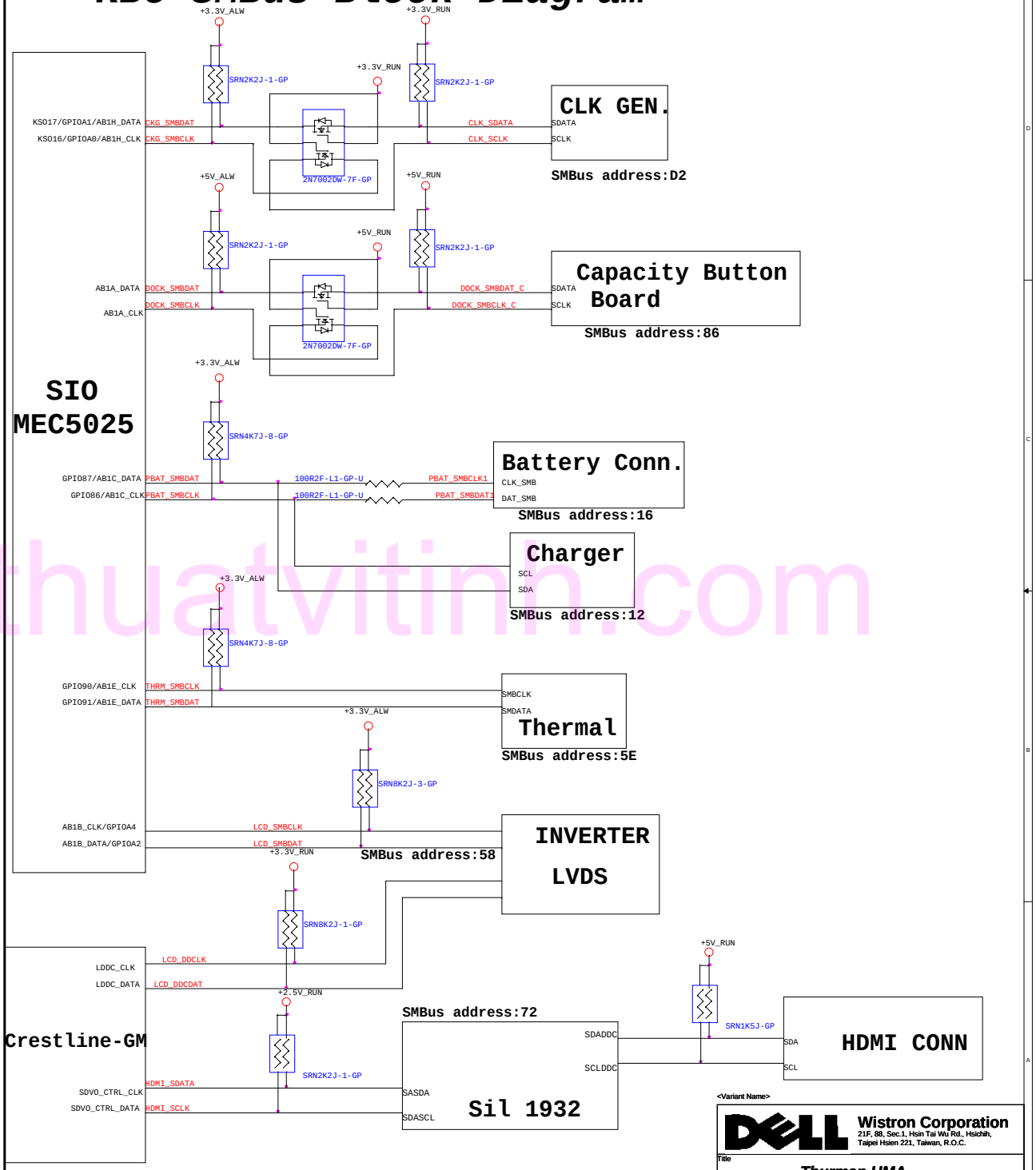
ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



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CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15
IO_VOUT[2,1,0]

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	TP3	AZ_DOUT_ICH	Description
0	0		RSVD
0	1		Enter XOR Chain
1	0		Normal Operation(default)
1	1		Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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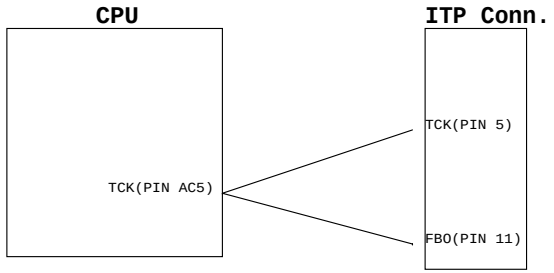

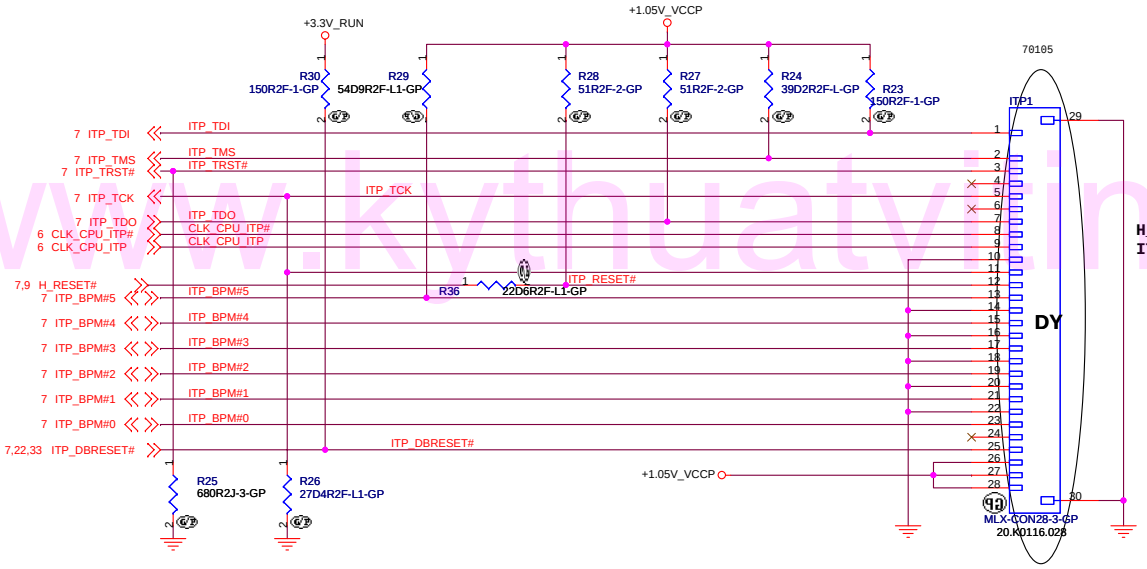

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max)

+1.05VRUN use Decoupling Capacitor close
ITP connector 100 mil (max)

ITP Debug Conn.

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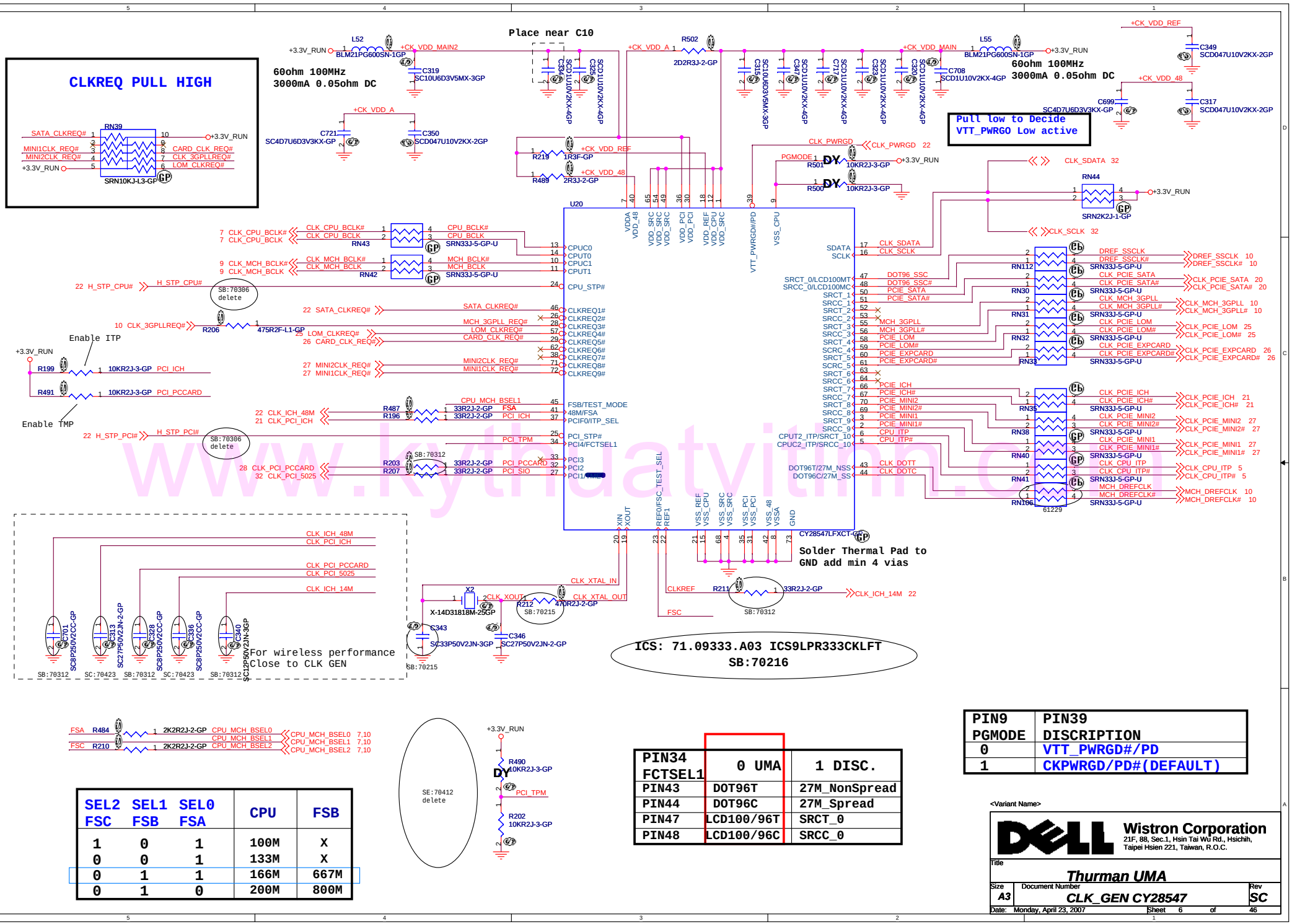

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

PIN9 PGMODE	PIN39 DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#(DEFAULT)

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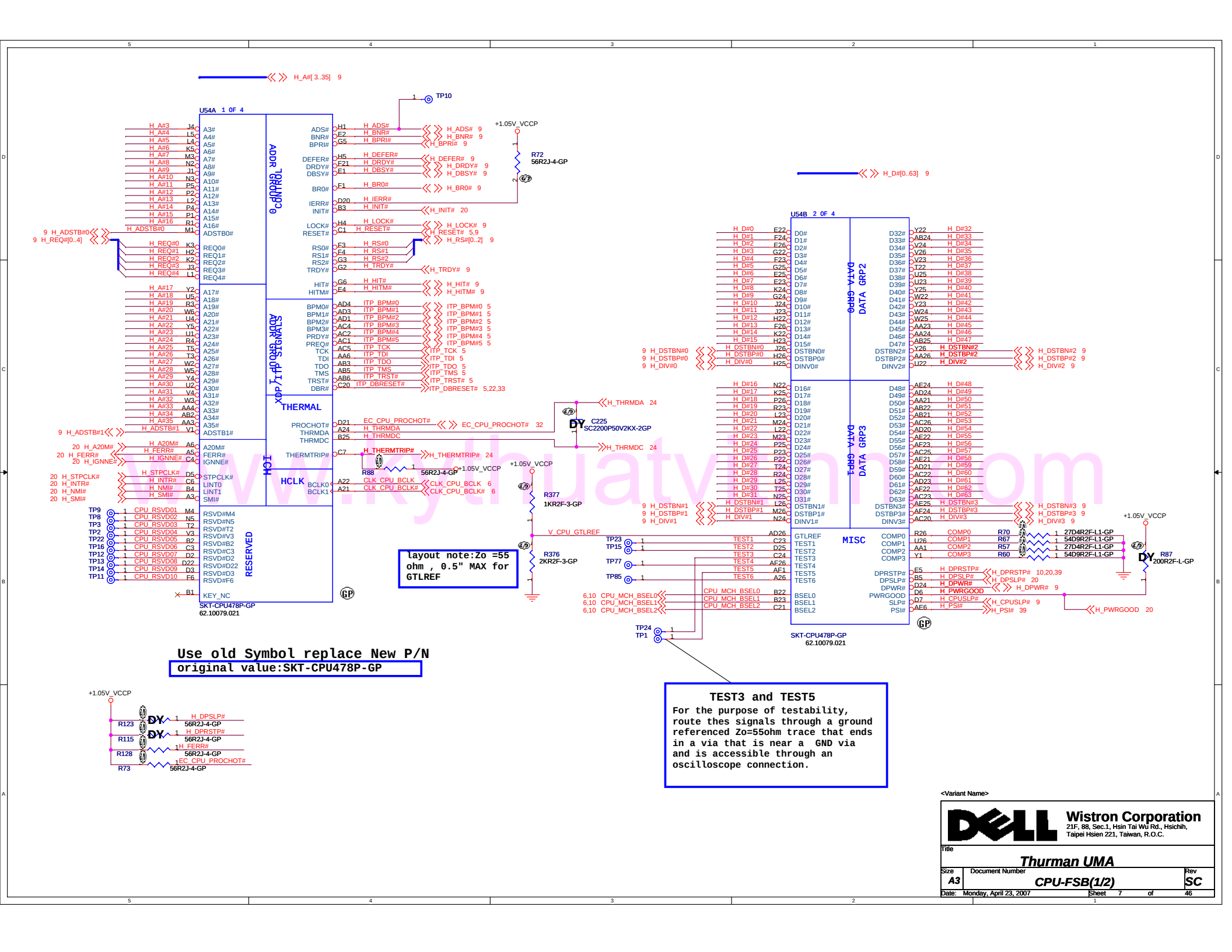
U54A 1 OF 4
U54B 2 OF 4
ADDR GROUP 0
ADDR GROUP 1
THERMAL
HCLK
RESERVED
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
SKT-CPU478P-GP
62.10079.021
TP10
R72 56R2J-4-GP
R88 56R2J-4-GP
R377 1KR2F-3-GP
R376 2KR2F-3-GP
C225 SC2200P50V2KX-2GP
R87 200R2F-L-GP
layout note:Zo =55 ohm , 0.5" MAX for GTLREF
Use old Symbol replace New P/N
original value:SKT-CPU478P-GP
TEST3 and TEST5
For the purpose of testability, route thes signals through a ground referenced Zo=55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.
R123 56R2J-4-GP
R115 56R2J-4-GP
R128 56R2J-4-GP
R73 56R2J-4-GP
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CPU-FSB(1/2)
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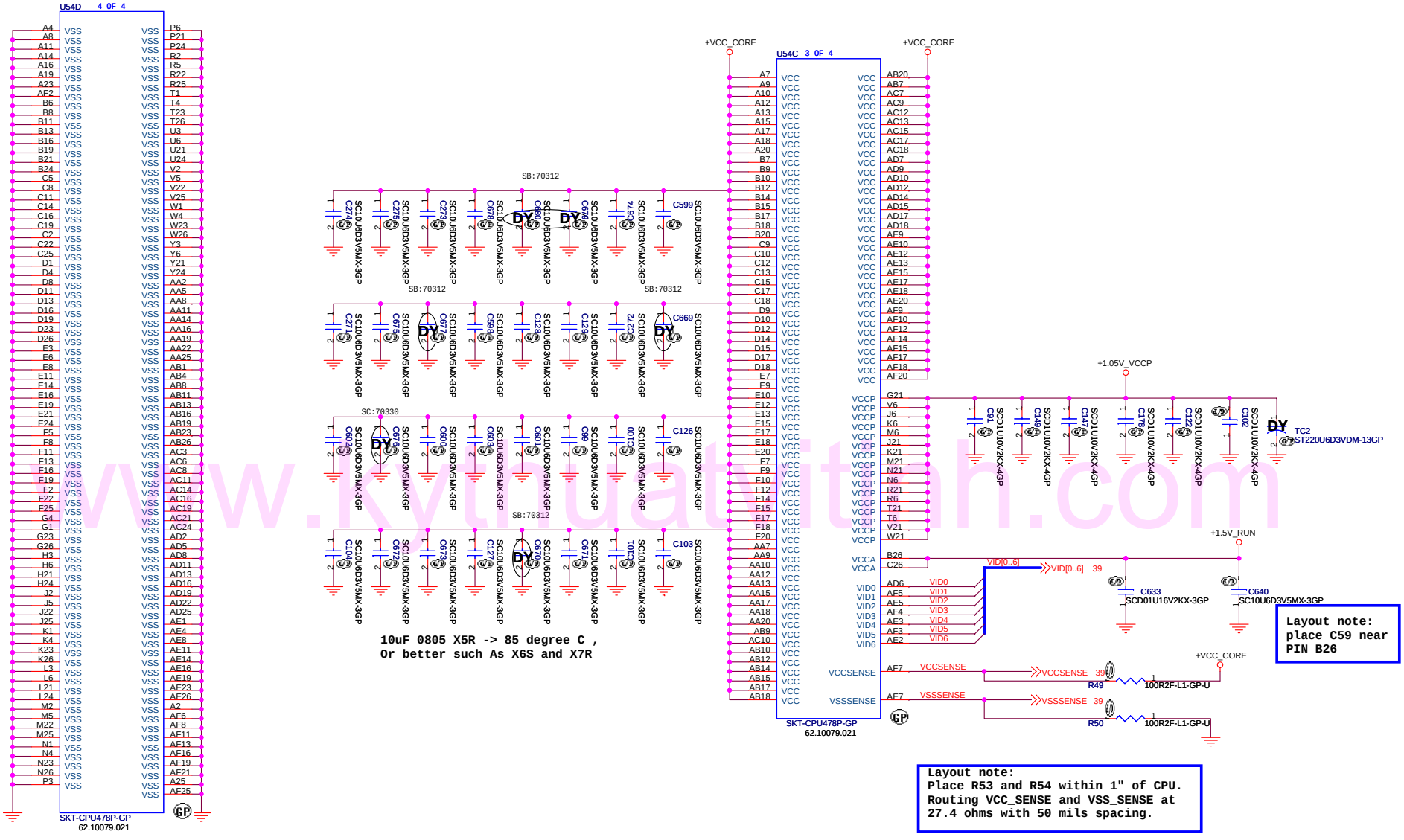

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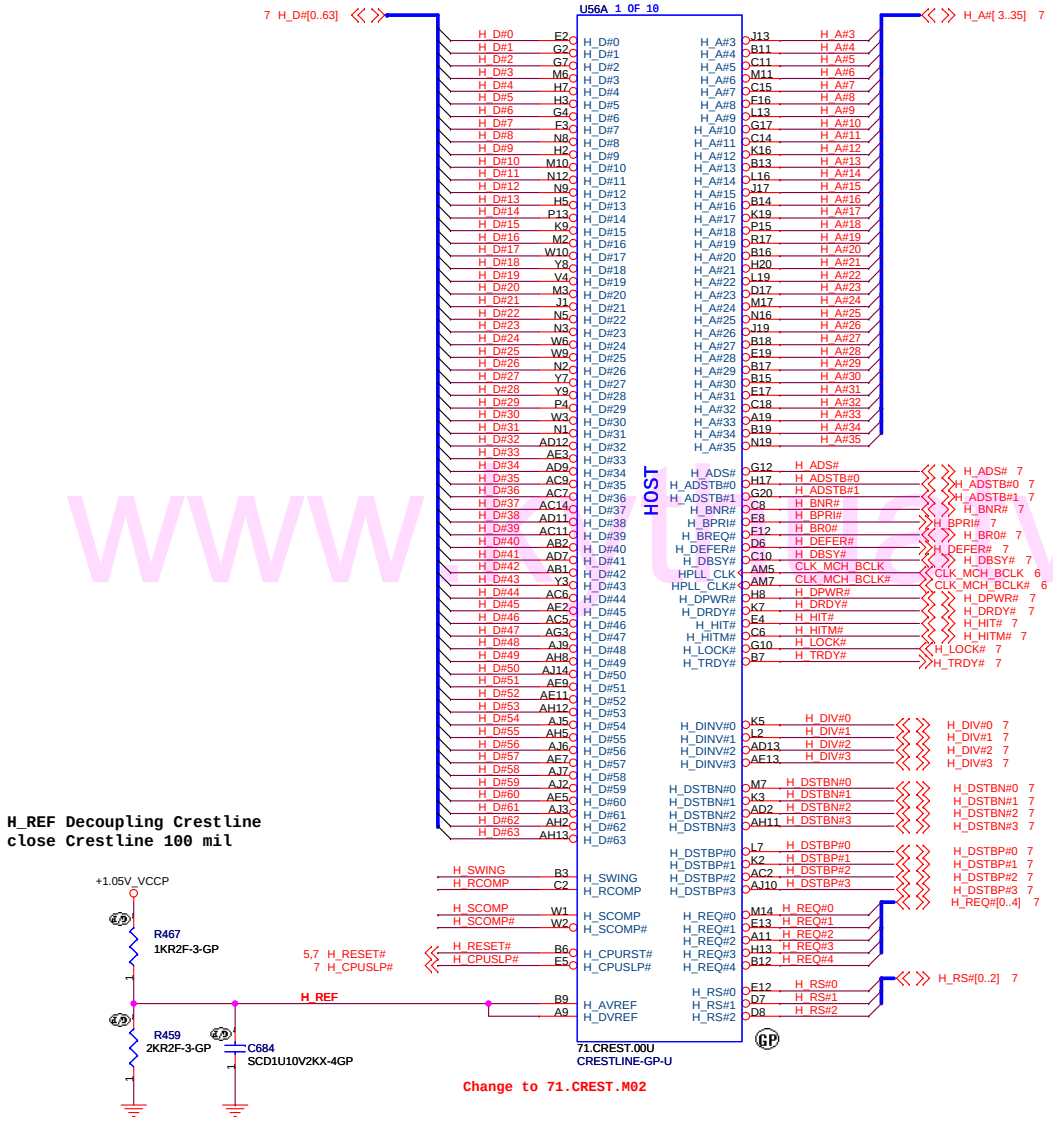


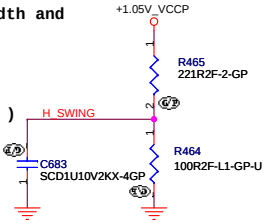
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close Caliistoga 500 mil (MAX)

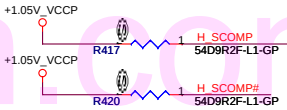
From Schematic Design Checklit v.1201

221 1% pull high 100

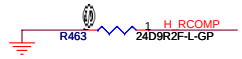
1% pull low



H_SCOMP and H_SCOMP# Resistors and Capacitors close Caliistoga 500 mil (MAX)
Zo=55ohms



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



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* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *
	CFG[2..0] FSB Select
LHL	FSB 800
LHH	FSB 667
Other	Reserved

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

Layout Note:
MCH_CLVREF ~= 0.350V
Width/Spacing = 12/12

CLOSE PIN BL15 BK14

U56B 2 OF 10

CRESTLINE-GP-U 71.CREST.00U

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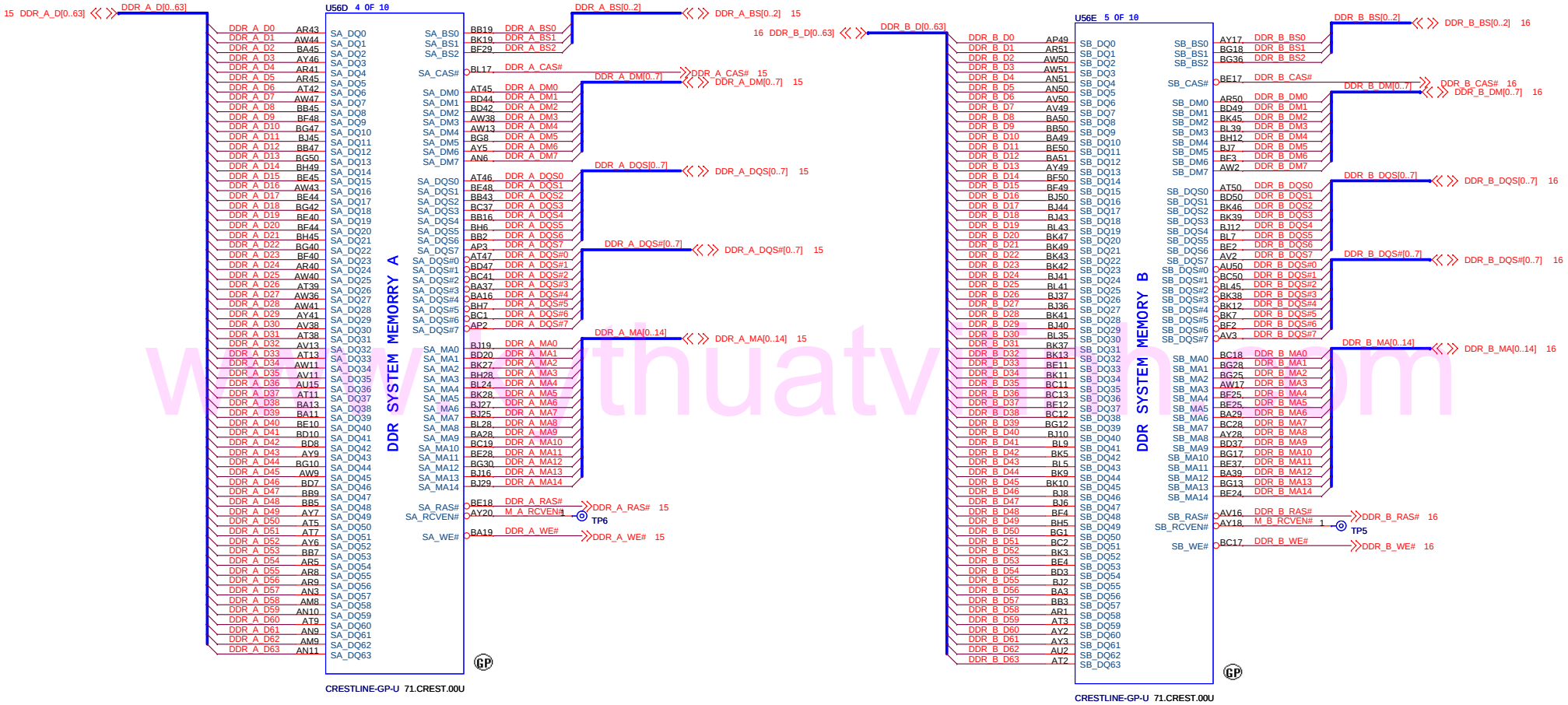

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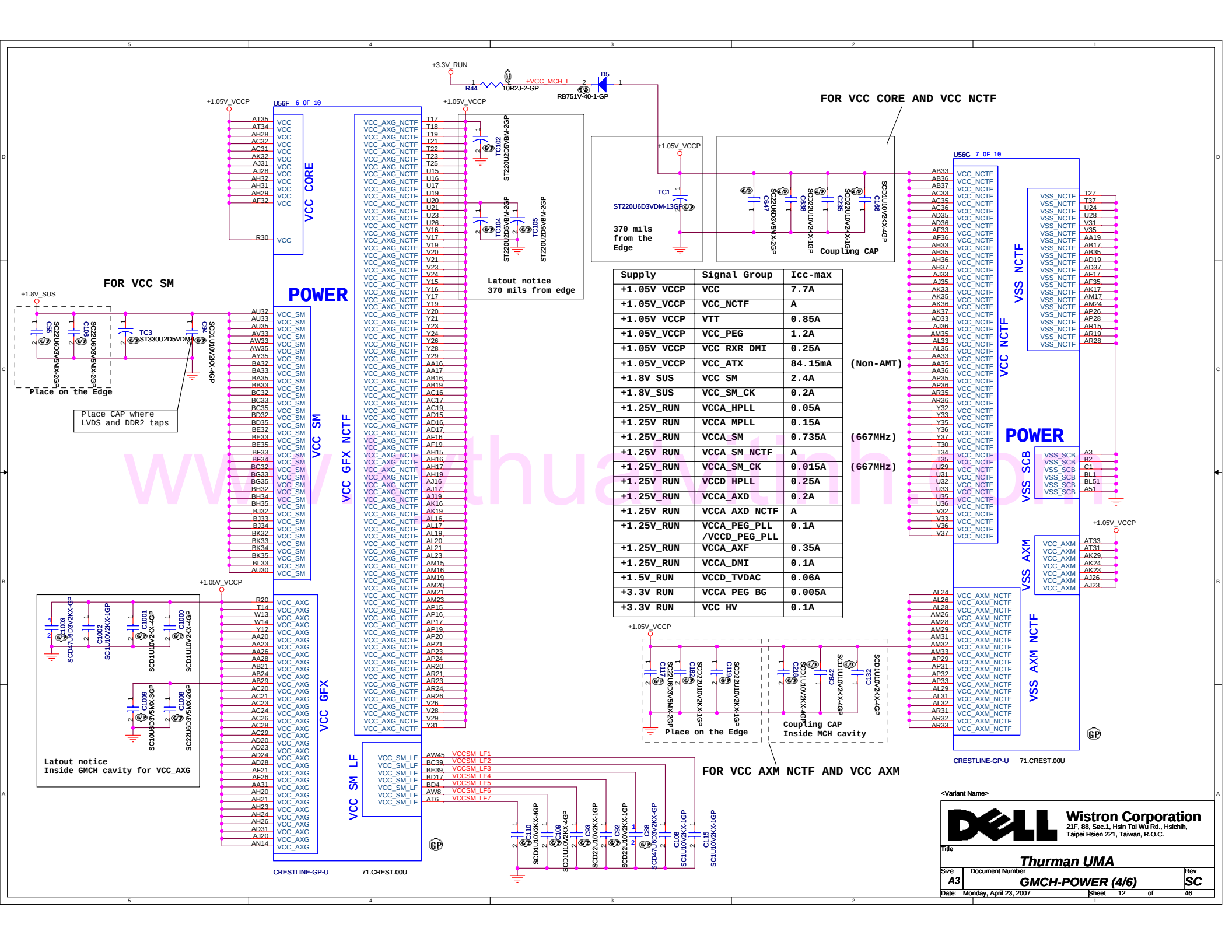

Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	7.7A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

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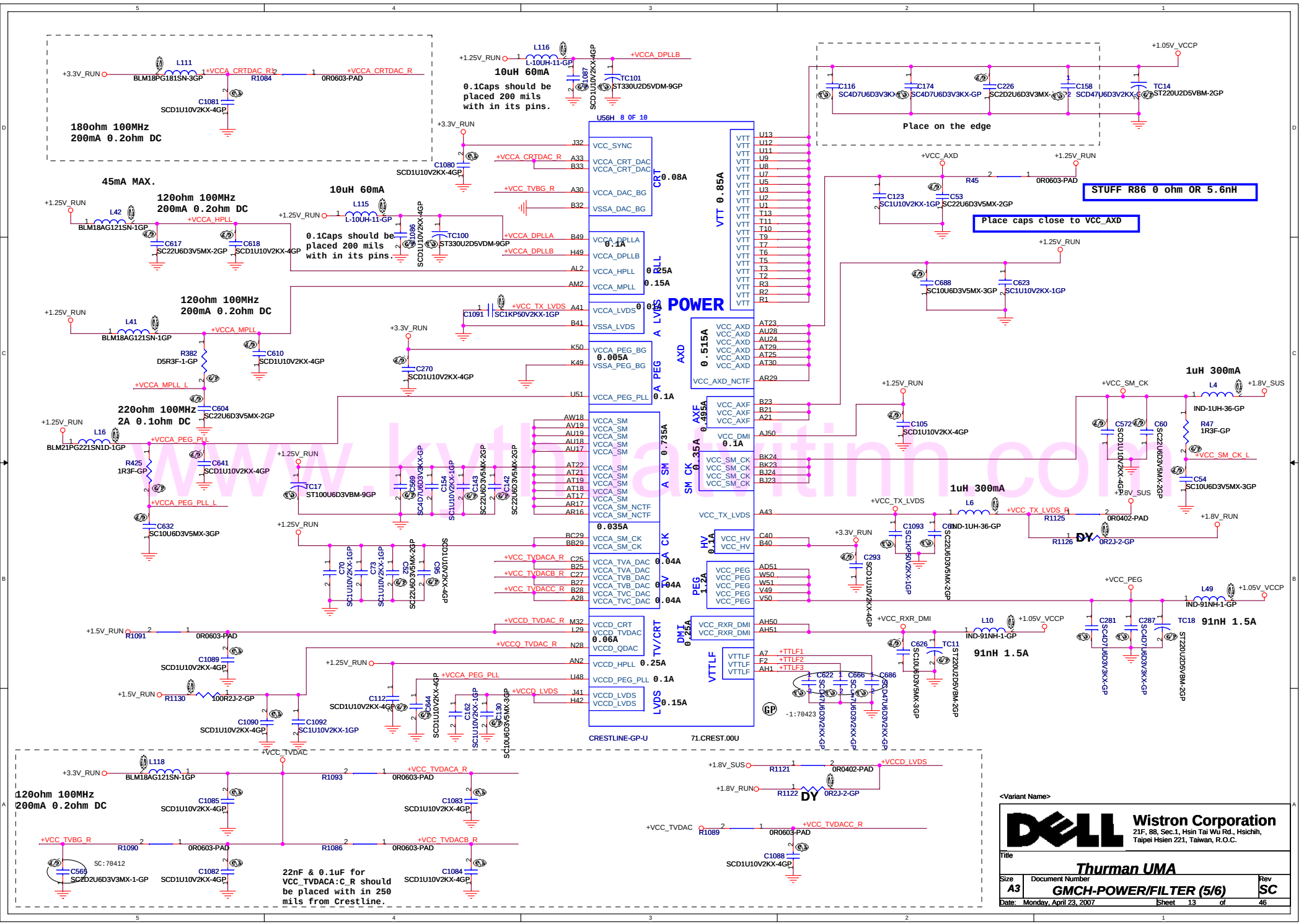
180ohm 100MHz
200mA 0.2ohm DC
45mA MAX.
120ohm 100MHz
200mA 0.2ohm DC
10uH 60mA
0.1Caps should be placed 200 mils with in its pins.
120ohm 100MHz
200mA 0.2ohm DC
220ohm 100MHz
2A 0.1ohm DC
120ohm 100MHz
200mA 0.2ohm DC
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.
Place on the edge
STUFF R86 0 ohm OR 5.6nH
Place caps close to VCC_AXD
1uH 300mA
1uH 300mA
91nH 1.5A
POWER
CRESTLINE-GP-U
71.CREST.00U
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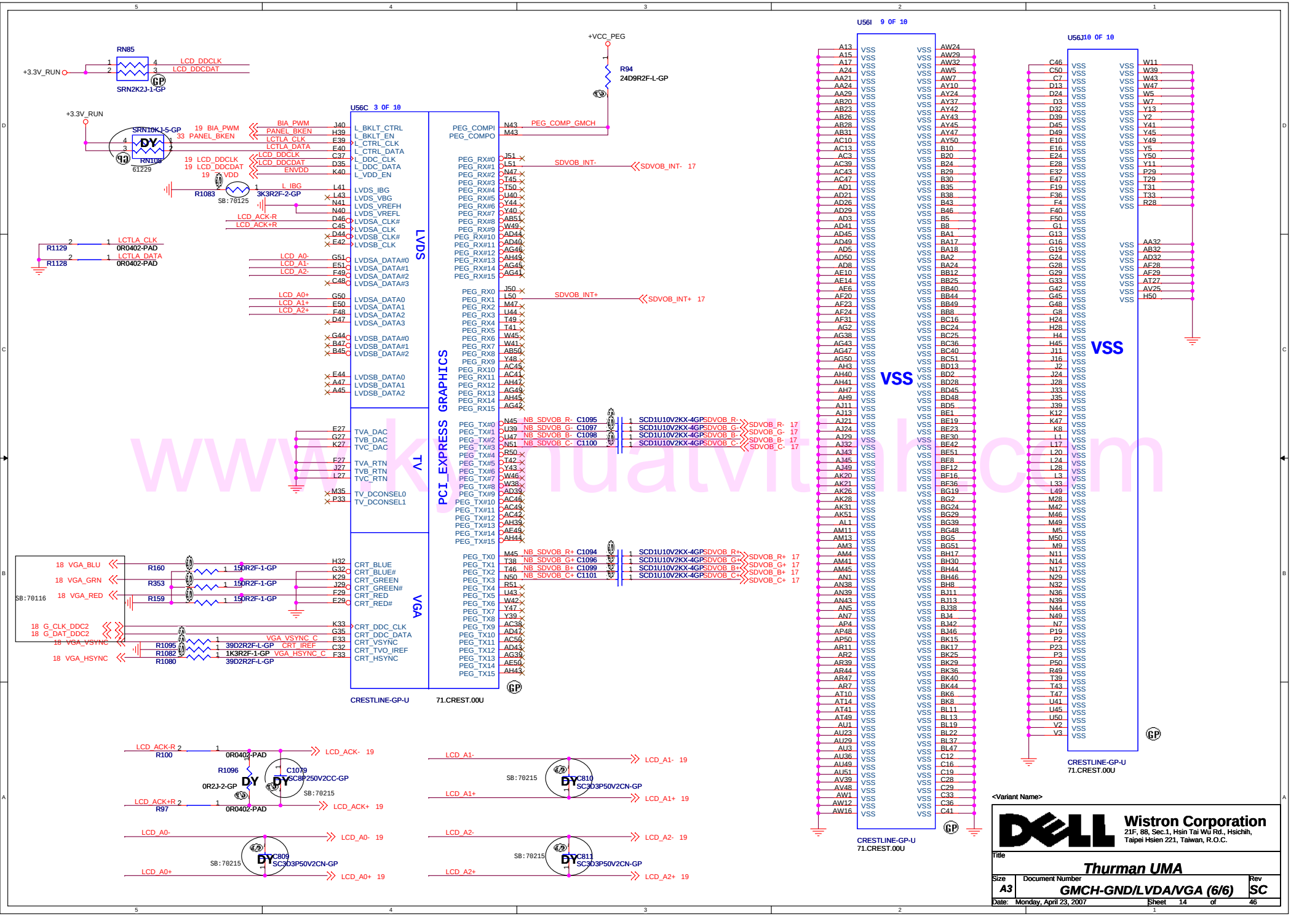
Thurman UMA
GMCH-POWER/FILTER (5/6)
Monday, April 23, 2007



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Title: Thurman UMA		
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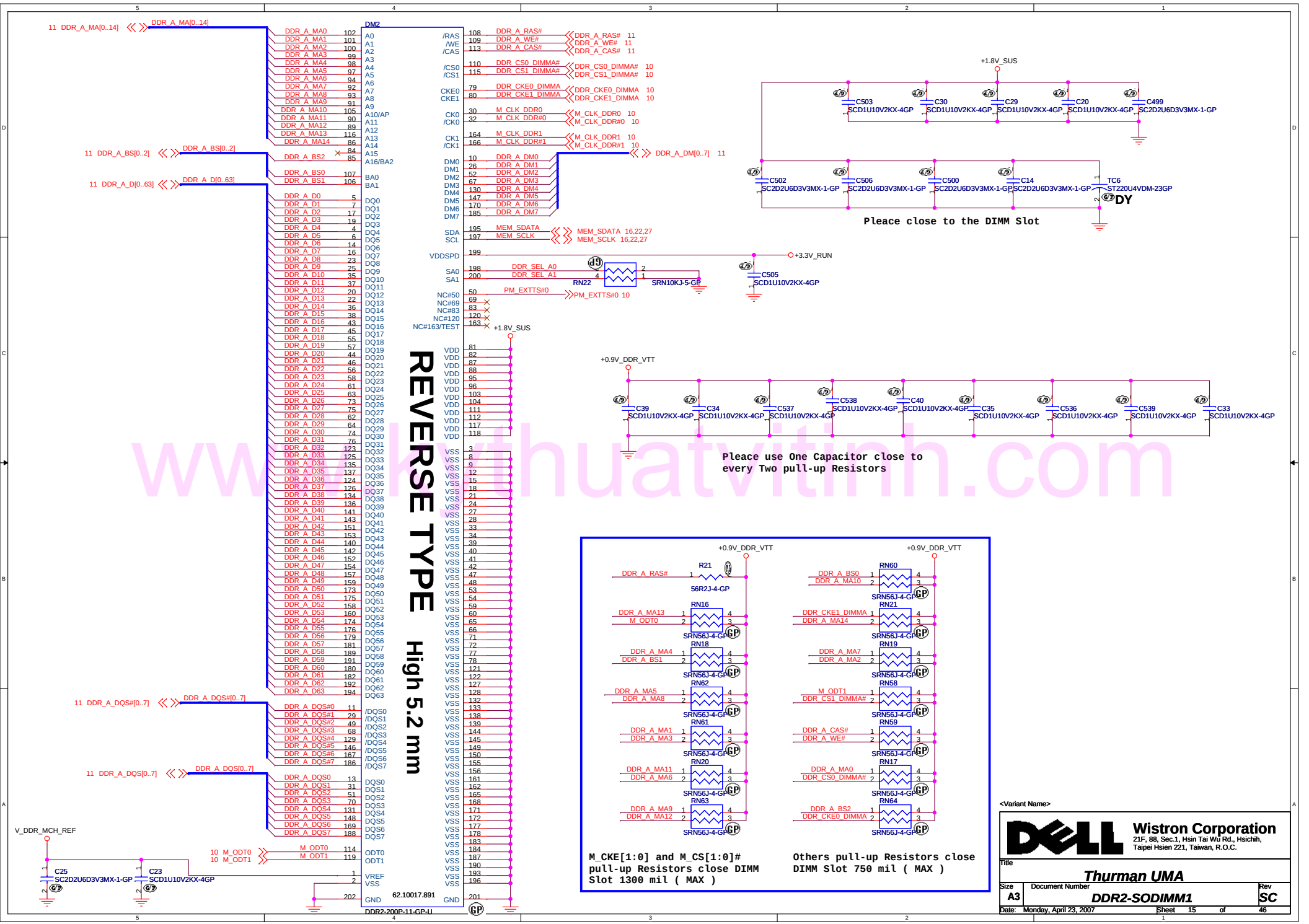

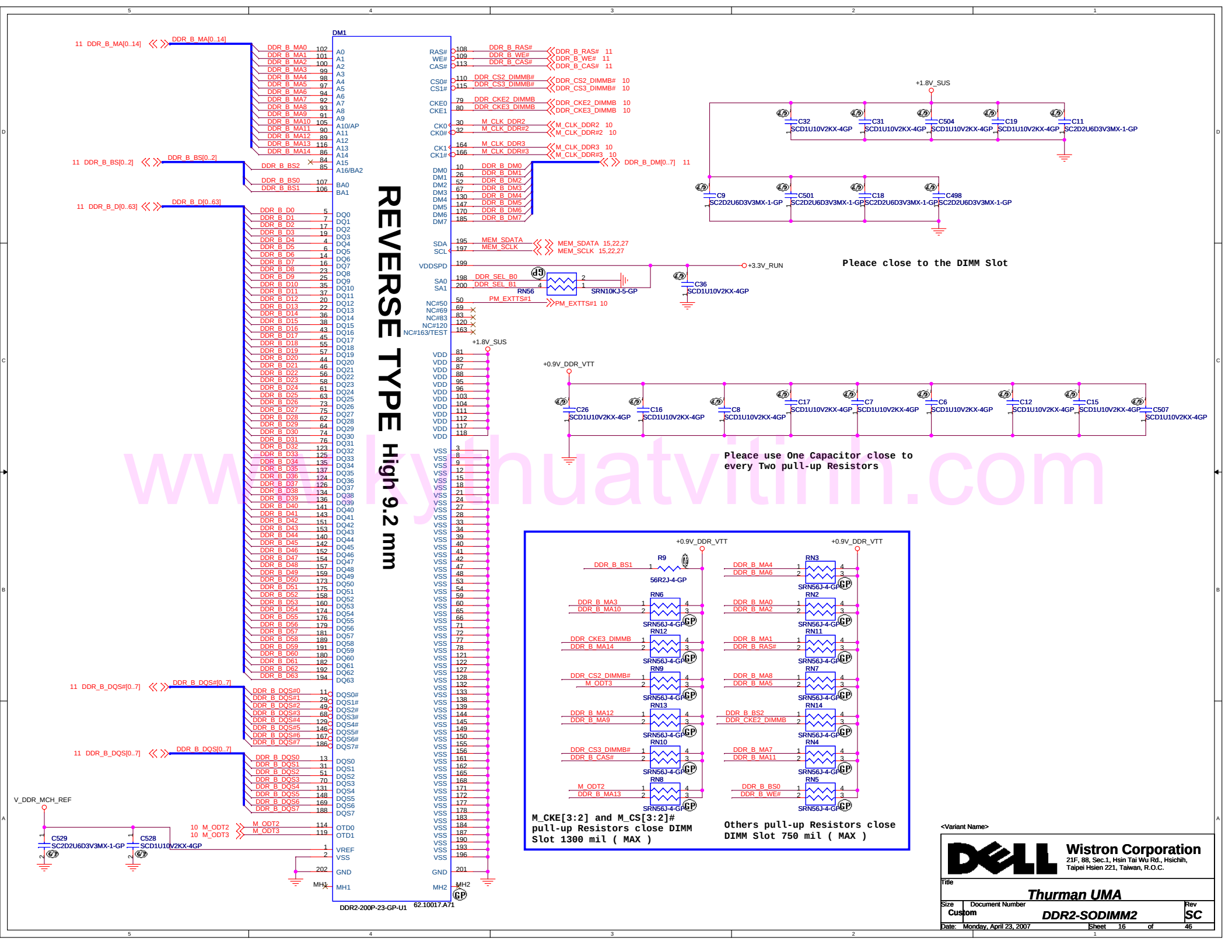
DM1
REVERSE TYPE High 9.2 mm
DDR2-200P-23-GP-U1
62.10017.A71
Please close to the DIMM Slot
Please use One Capacitor close to every Two pull-up Resistors
M_CKE[3:2] and M_CS[3:2]# pull-up Resistors close DIMM Slot 1300 mil (MAX)
Others pull-up Resistors close DIMM Slot 750 mil (MAX)
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Thurman UMA
DDR2-SODIMM2
Custom
SC
Monday, April 23, 2007
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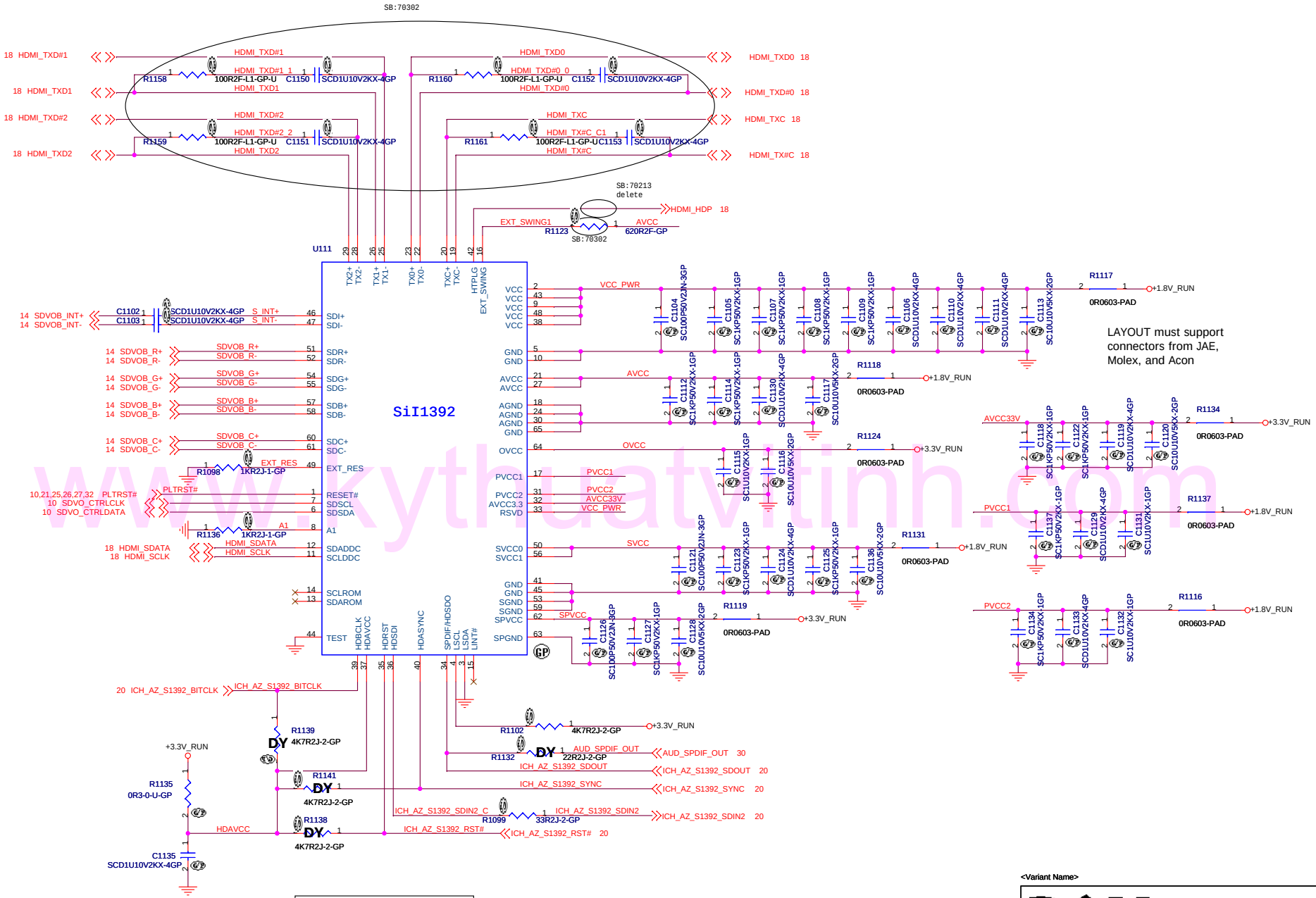
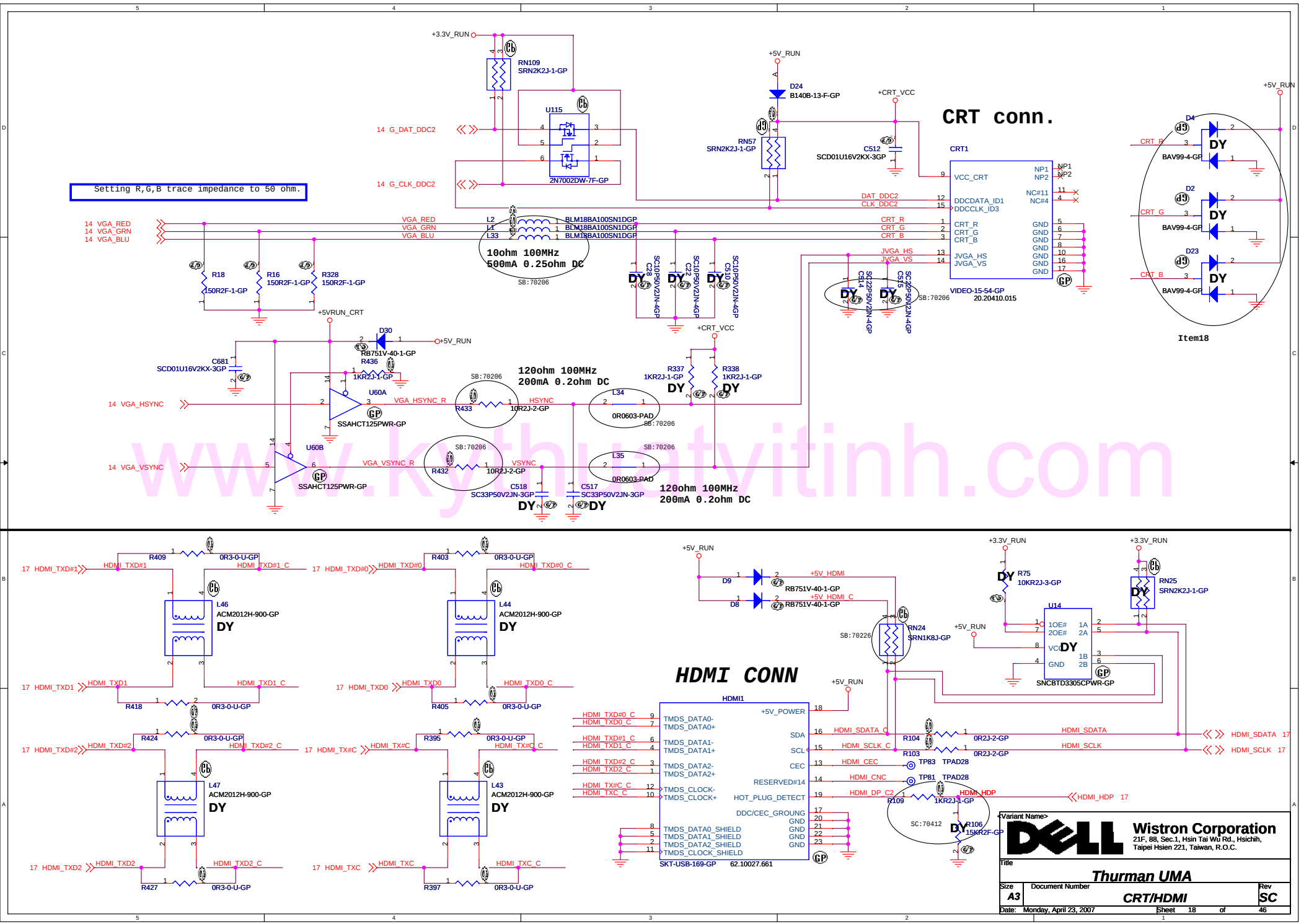
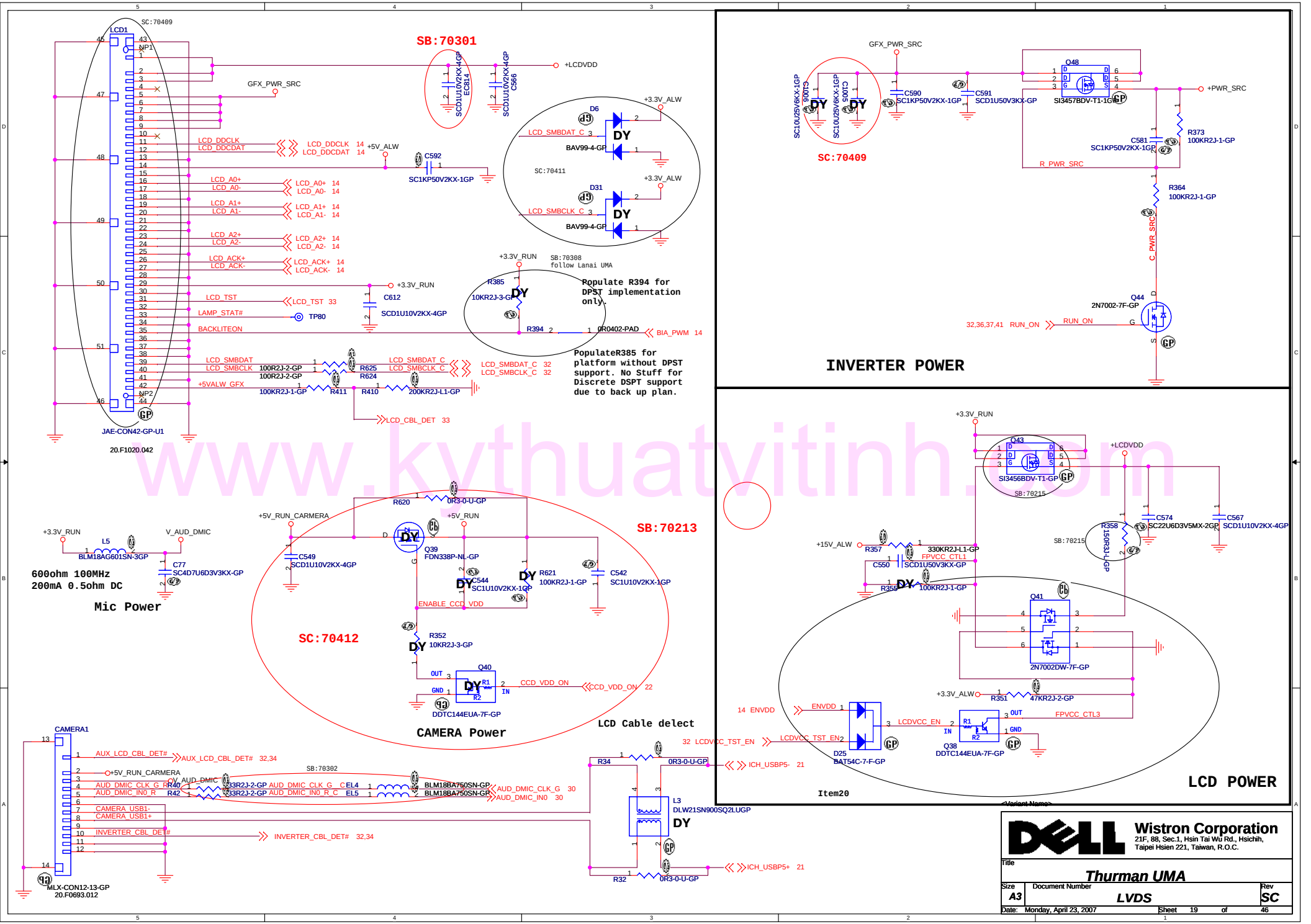






We would like to change X5 to 82.10026.021 and X3 to 82.30001.691.

RTC circuitry

SC:70412T

ICH8-Strap PIN

integrated VccSus1_05,VccSus1_5,VccCL1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable

This circuit is only needed if the platform has the SNIFFER

Distance between the ICH8-M and cap on the "P" signal should be identical distance between the ICH8-M and cap on the "N" signal for same pair.

SM_SATASB Place within 500 mil of ICH8-M

GLAN_COMP place within 500 mil of ICH8M

ICH8-Strap PIN

XOR Chain Entrance Strap		
ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

ICH8-M-1-GP-U 71.0ICH8.A0U

IC SB ICH8M QM74 MM#882553 B0

Change to 71.0ICH8.M08

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA

Size: A3 | Document Number: ICH8M-RTC/IDE/LPC/DHI (1/4) | Rev: SC

Date: Monday, April 23, 2007 | Sheet 20 of 46

ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

PCI I/F PULL HIGH

BIOS should not enable the internal GPIO pull up

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

PCI Interface Routing

Add Buffers as need for Loading and Fanout concerns

CLK_ICH_14M EMI Mode Place close to ICH8-M

EMI

DMI_COMP R158 place within 500 mil of ICH8M

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	MINI Card WLAN
USB9	

PCIE Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard MINI
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	LAN

Layout Note:
Place R235, R237 and R234 within 500 mils from ICH.

USBRBIAS close to ICH8M 500 mils and Trace impedance should be 60 ohm +/- 15%

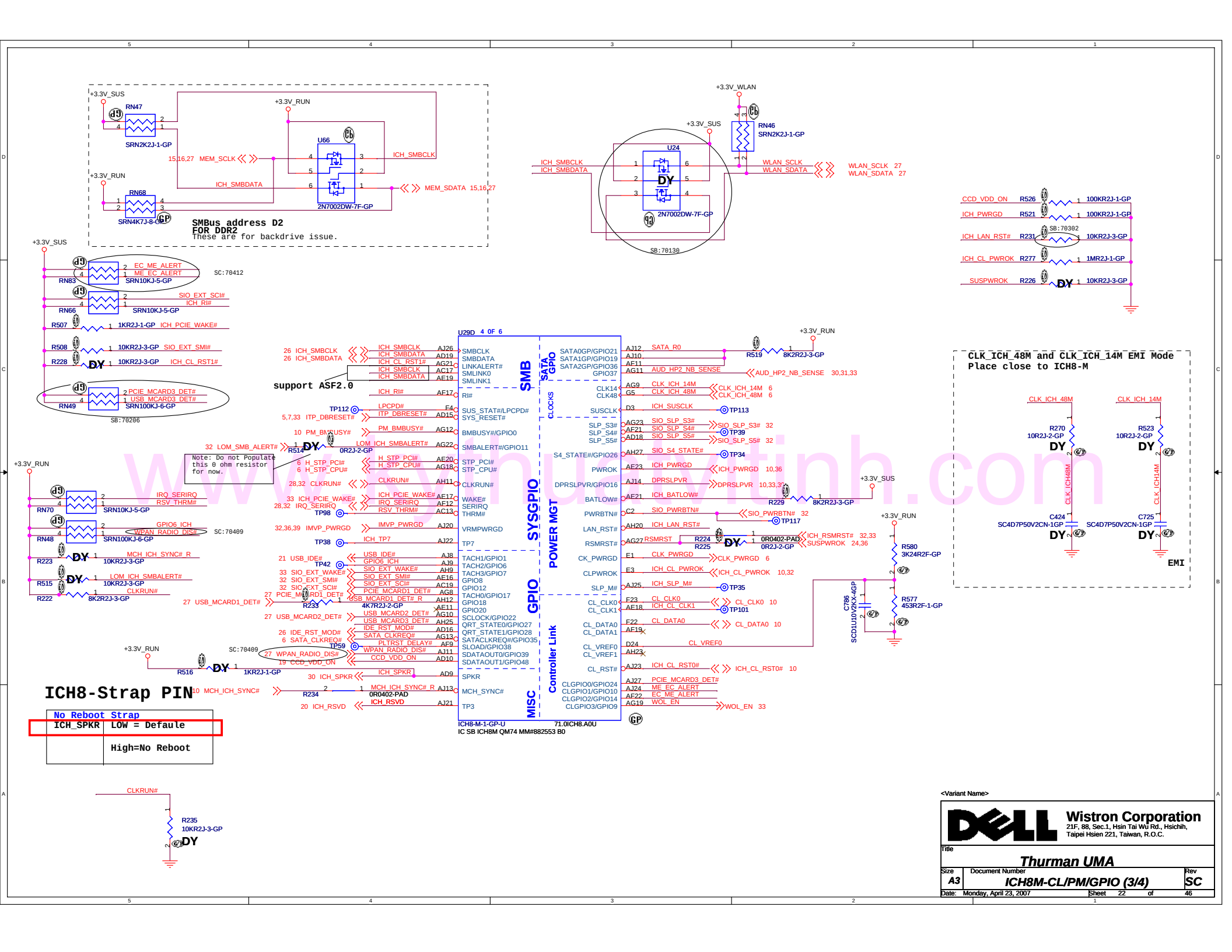
<Variant Name>

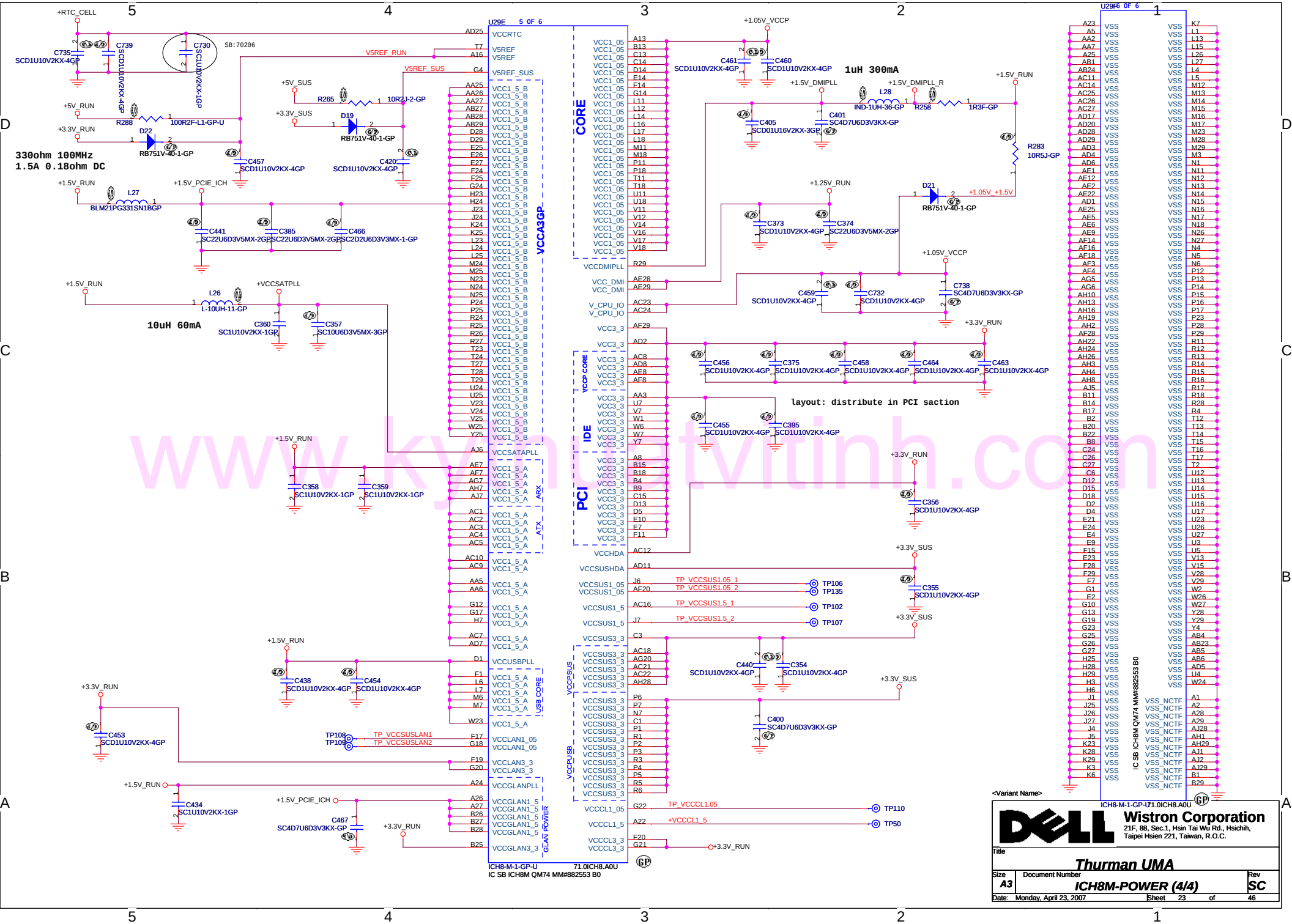
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA

Size: A3 | Document Number: ICH8M-PCIE/USB/SPI/DMI (2/4) | Rev: SC

Date: Monday, April 23, 2007 | Sheet 21 of 46


SMBus address D2
FOR DDR2
These are for backdrive issue.
support ASF2.0
Note: Do not Populate this 0 ohm resistor for now.
CLK_ICH_48M and CLK_ICH_14M EMI Mode
Place close to ICH8-M
ICH8-Strap PIN
No Reboot Strap
ICH_SPKR LOW = Defaule
High=No Reboot
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
ICH8-M-1-GP-U
IC SB ICH8M QM74 MM#882553 B0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Thurman UMA
ICH8M-CL/PM/GPIO (3/4)
Monday, April 23, 2007



SSID = THERMAL

REM_DIODE1_N and REM_DIODE1_P routing Trace width and Spacing use 10 / 10 mil

Place inside CPU socket

C300 Please close to Guardian

C295 Please close to Guardian

H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

C276 Please Close to Guardian

Place near the bottom SODIMM CONN

REM_DIODE4_N and REM_DIODE4_P routing Trace width and Spacing use 10 / 10 mil

Thermal sensor for Mini Card should be placed TOP Side under WWAN CARD

C260 Please Close to Guardian

Close to Pin5, Pin6

Close to Pin9

U16

EMC4001-HZH-1GP

Version B: 74.04001.A73

Note :

VSET = (Tp - 70) / 21
3.3 * (R411/ R406 + R411) = (Tp - 70) / 21
Where Tp = 70 to 101 degrees C
Tp set at 88 degrees C
Guardian temp tolerance = +/- 3 degrees C

should be placed BOT DIMM

pull up on SIO

CPU THERMALTRIP

MCH THERMALTRIP

C916, C459, C472 Please Close to Guardian

Wistron Corporation
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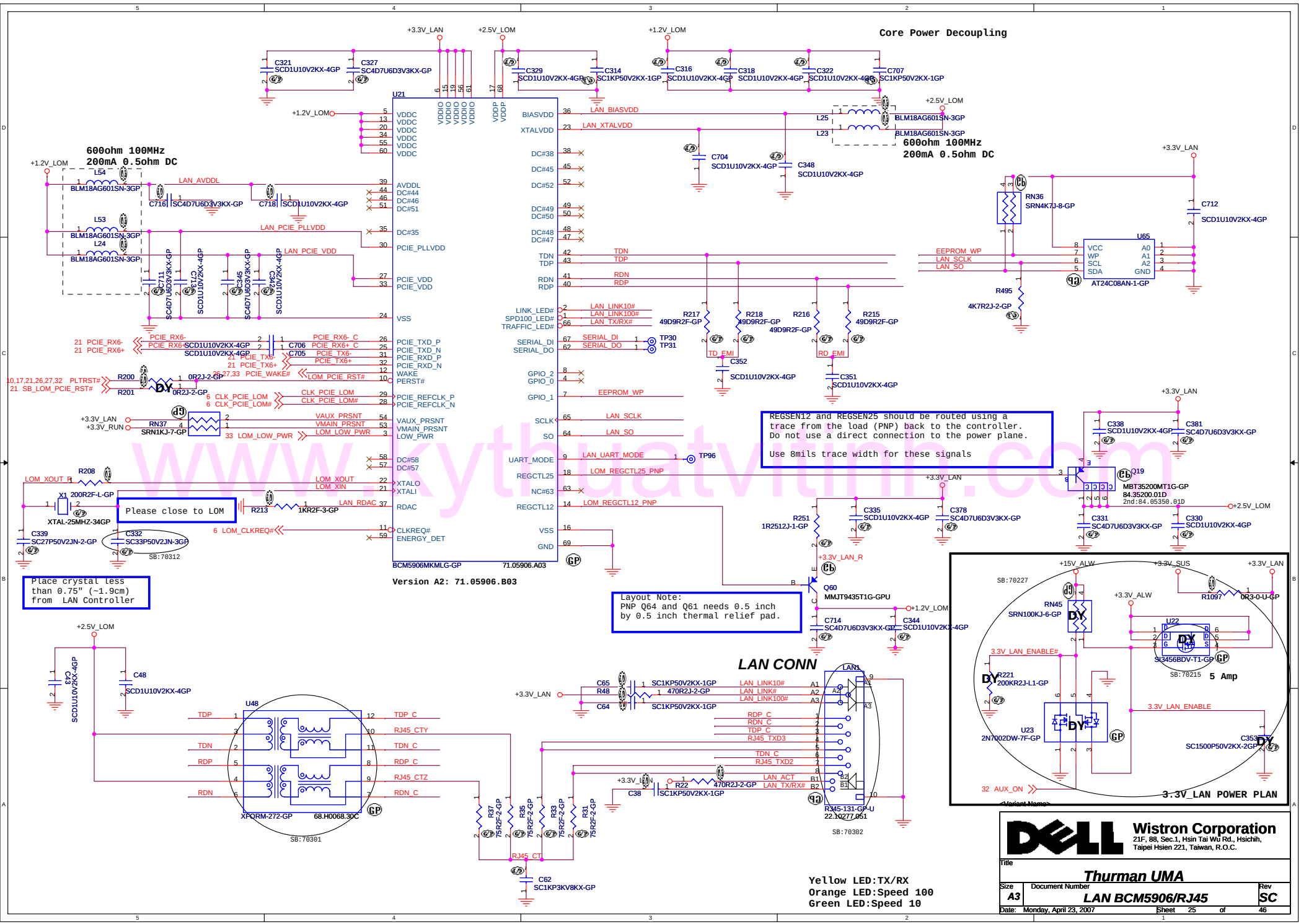
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA

Size: A3 | Document Number: FAN/EMC4001 | Rev: SC

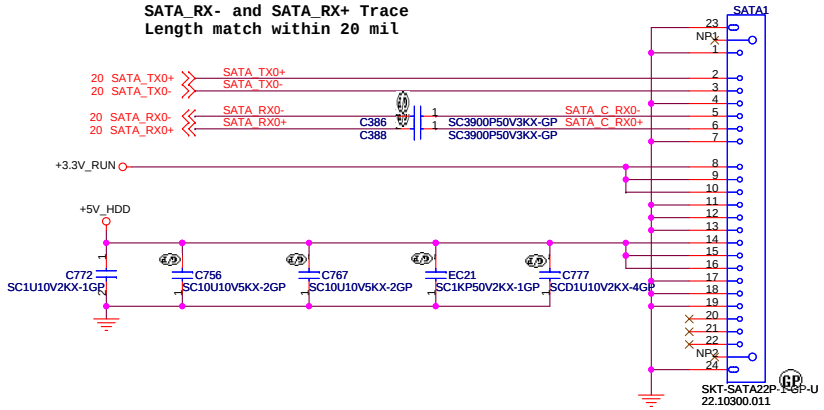
Date: Monday, April 23, 2007 | Sheet 24 of 46

<Variant Name>

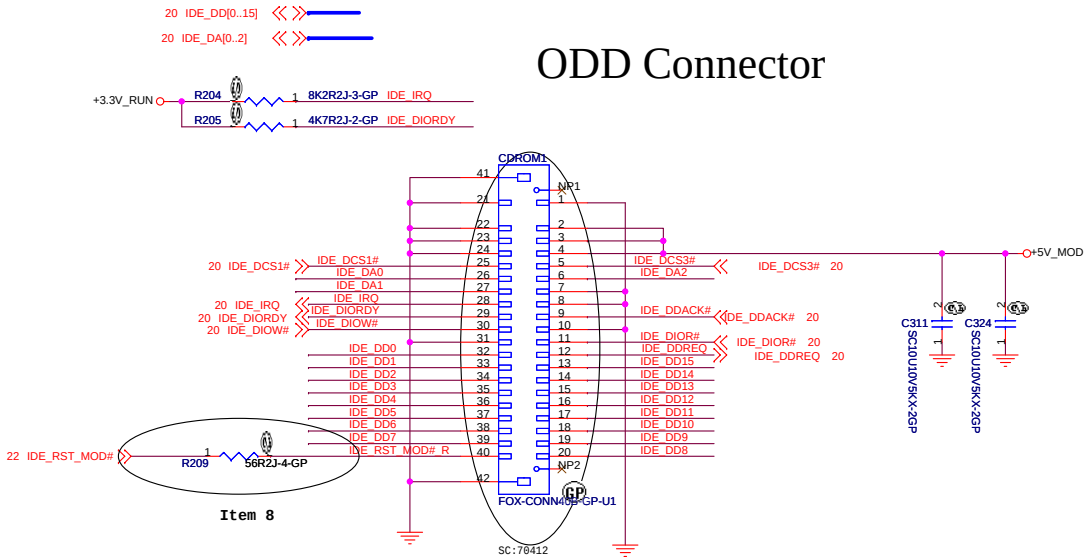

Core Power Decoupling
600ohm 100MHz
200mA 0.5ohm DC
600ohm 100MHz
200mA 0.5ohm DC
REGSEN12 and REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.
Use 8mils trace width for these signals
Please close to LOM
Place crystal less than 0.75" (~1.9cm) from LAN Controller
Layout Note: PNP Q64 and Q61 needs 0.5 inch by 0.5 inch thermal relief pad.
LAN CONN
Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10
Version A2: 71.05906.B03
BCM5906MKMLG-GP
71.05906.A03
XFORM-272-GP
68.H0068.30C
SB:70301
SB:70302
SB:70312
SB:70215
SB:70227
5 Amp
3.3V_LAN POWER PLAN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Thurman UMA
LAN BCM5906/RJ45
Size A3
Rev SC
Date: Monday, April 23, 2007
Sheet 25 of 46

SSID = IDE & SATA

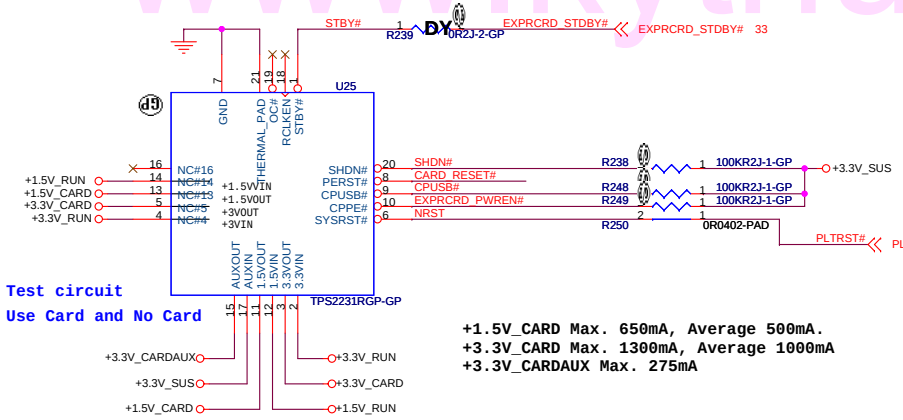
SATA HDD Connector



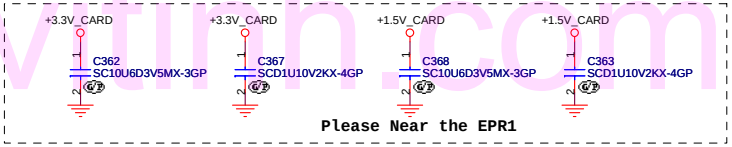
ODD Connector

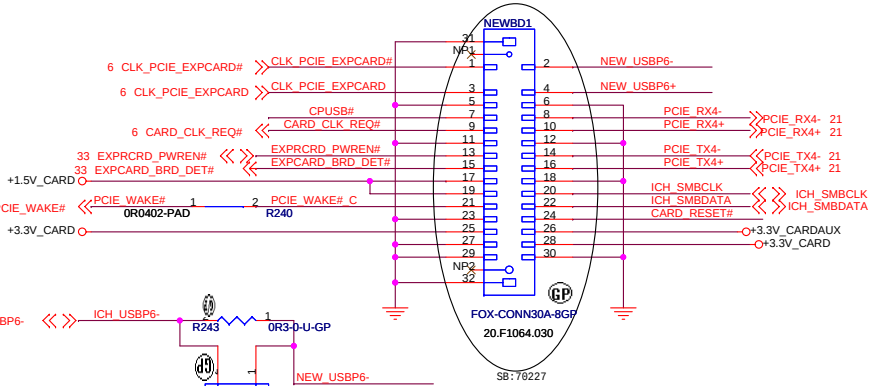


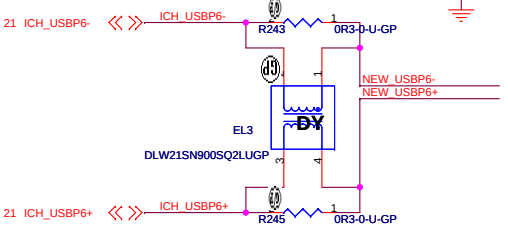
Express Card

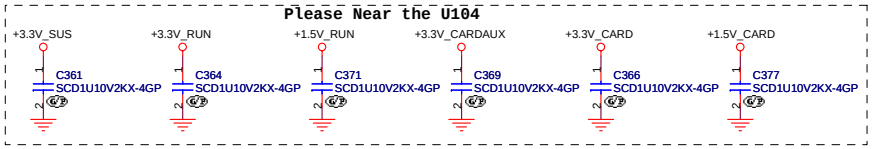


+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA









<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thurman UMA***

Size	Document Number	Rev
A3	HDD/ODD/TO EXPRESS BD CONN	SC

Date: Monday, April 23, 2007 Sheet 26 of 46

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

DEBUG PINS

MiniCard WLAN connector

MiniCard WWAN connector

Prevent backdrive when WoW is enabled.

C587 Please Near the MINICARD1/Pin24

This circuit is only needed if the platform has the SNIFFER

SB:070301

For Debug card used only.

Layout note: Place caps EC10-EC14 close Mini Card connector.

C337 Please Near the MINICARD2/Pin24

Close WLAN1

SC:70409

Layout note: Place caps EC87,EC88 close SIM Card connector.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

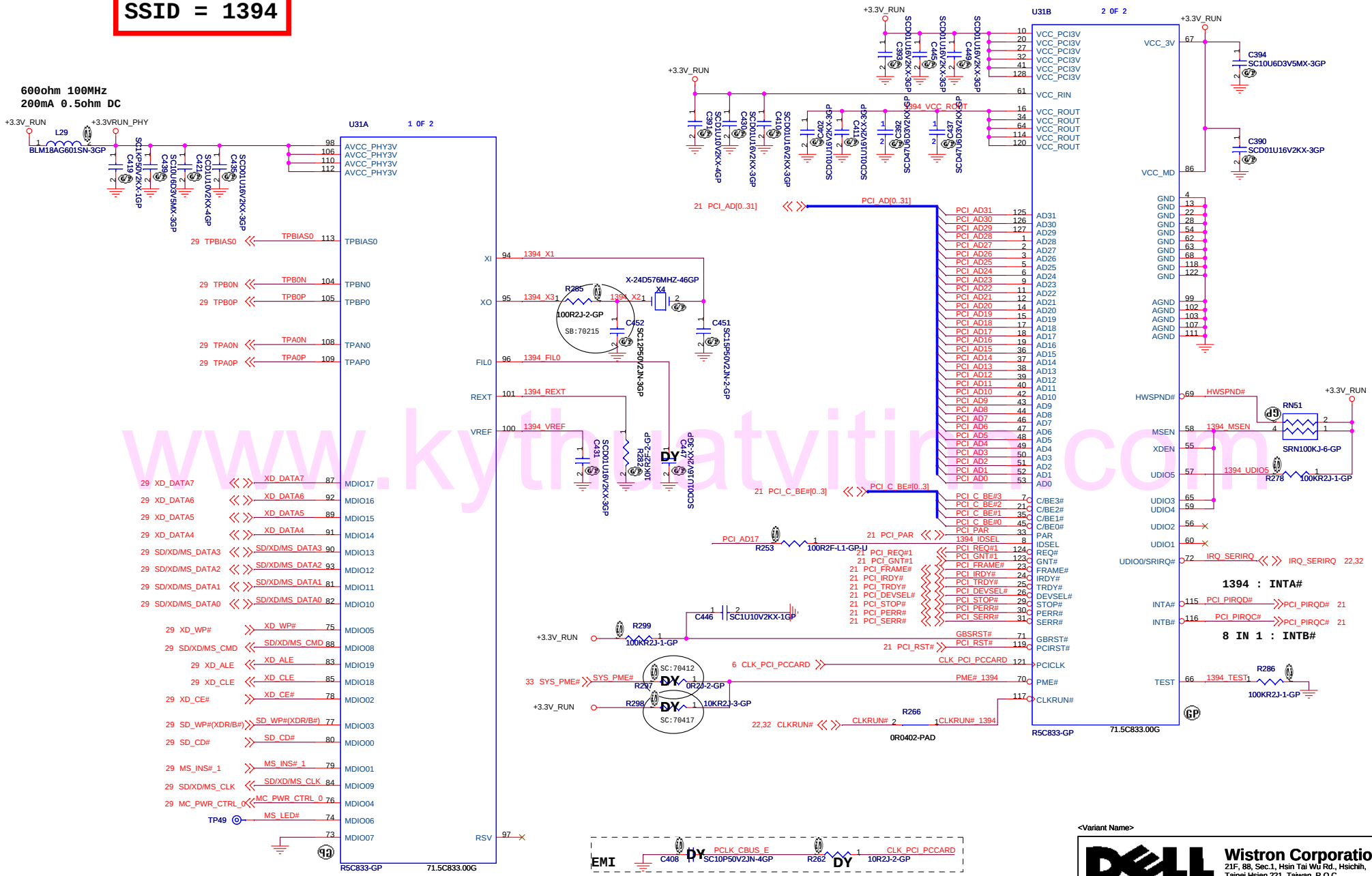
Title: Thurman UMA

Size: A3 | Document Number: MINICARD/WLAN/WWAN | Rev: SC

Date: Monday, April 23, 2007 | Sheet 27 of 46

SSID = 1394

600ohm 100MHz
200mA 0.5ohm DC



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

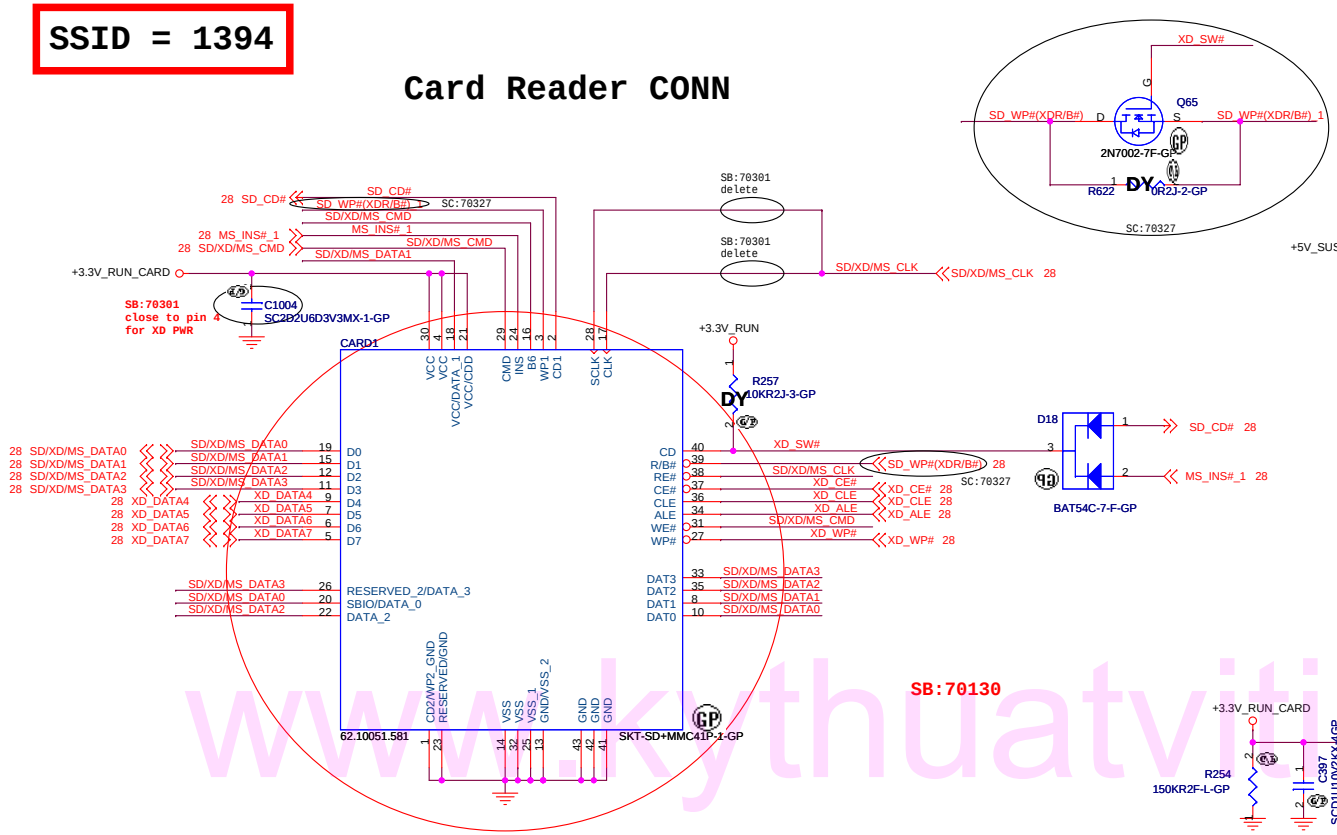
Title: Thurman UMA

Size	Document Number	Rev
A3	1394 R5C833	SC

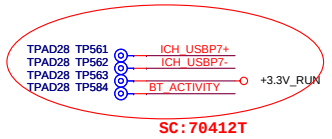
Date: Monday, April 23, 2007 Sheet 28 of 46

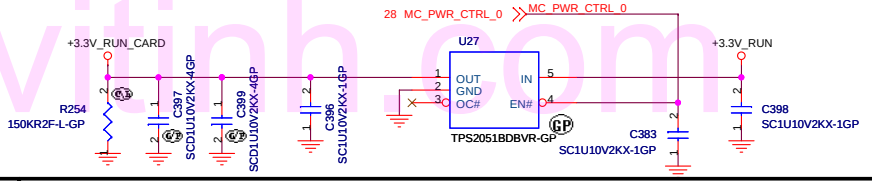
SSID = 1394

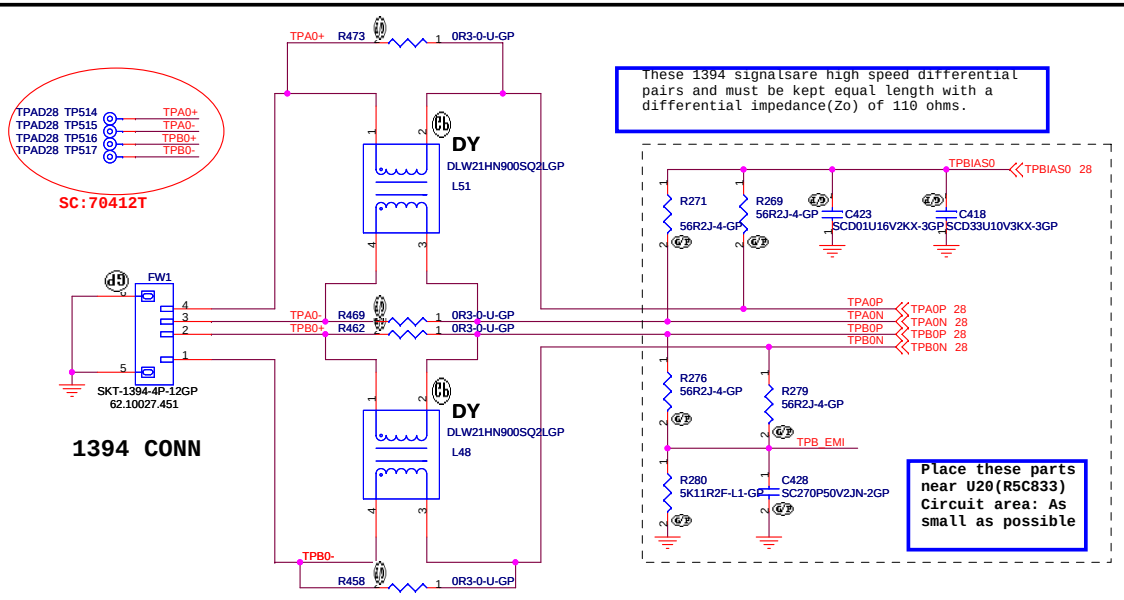
Card Reader CONN



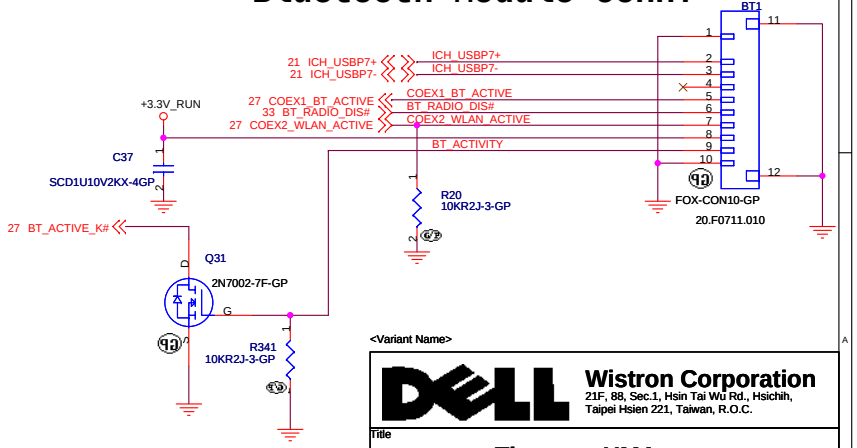
SNIFFER BOARD CONN







Bluetooth Module conn.



<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Thurman UMA		
Size: A3	Document Number: 8in1 /1394/SNIFFER BD CON/BT	Rev: SC
Date: Monday, April 23, 2007	Sheet 29 of 46	

60ohm 100MHz
3000mA 0.05ohm DC

+3.3V_RUN
L60 BLM21PG600SN1-GP
+3V_RUN_DVDD_CORE
C783 SCD1U10V2KX-4GP
C450 SCD1U10V2KX-4GP
C791 SC1U10V2KX-1GP
R284 100KR2J-1-GP
+3V_RUN_DVDD_CORE3
C448 SC1KP50V2KX-1GP

U76
DVDD_CORE
DVDD_CORE
DVDD
BIT_CLK
SDATA_IN
SDATA_OUT
SYNC
RESET#
AVDD1
AVDD2
SENSE_A
SENSE_B
PORT_A_L
PORT_A_R
VREFOUT_A
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
VREFOUT_D
PORTE_L
PORTE_R
VREFOUT_E
PORTF_L
PORTF_R
VREFOUT_F
PORTG_L
PORTG_R
PORTH_L
PORTH_R
CD_L
CD_GND
CD_R
PC_BEEP
CAP2
VREFFILT
AVSS1
AVSS2
VOLUME UP/DMIC_0/GPIO1
VOLUME DN/DMIC_1/GPIO2
SPDIF_IN/GPIO0/DMIC_CLK
SPDIF_OUT
DVSS1
DVSS2
STAC9228X5TAEA2-GP
71.09228.00G

20 ICH_AZ_CODEC_BITCLK
20 ICH_AZ_CODEC_SDIN0
20 ICH_AZ_CODEC_SDOUT
20 ICH_AZ_CODEC_SYNC
20 ICH_AZ_CODEC_RST#
R583 33R2J-2-GP
SB_AZ_CODEC_SDIN0_R

+3.3V_RUN
U36 74LVC1G125DC-GP
19 AUD_DMIC_CLK_G
AUD_DMIC_CLK_G
R306 0R2J-2-GP
AUD_DMIC_CLK

19 AUD_DMIC_IN0
31 AUD_EAPD#
AUD_DMIC_IN0
AUD_EAPD#
R584 10KR2J-3-GP
AUD_DMIC_CLK
AUD_SPDIF_OUT
17 AUD_SPDIF_OUT

C770 SCD1U10V2KX-4GP
C436 SC1U10V2KX-1GP
+VDDA

AUD_SENSE_A
AUD_SENSE_B
AUD_HP1_OUT_L
AUD_HP1_OUT_R
AUD_HP1_OUT_L 31
AUD_HP1_OUT_R 31
TO Audio OP
AUD_LINE_OUT_L
AUD_LINE_OUT_R
AUD_LINE_OUT_L 31
AUD_LINE_OUT_R 31
TO Audio OP
AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_B
AUD_HP2_OUT_L 31
AUD_HP2_OUT_R 31

PORT C : LEAVE NC
IF NO INTERNAL MICS.

Port A---> HP1
Port E---> ext Mic
Port D---> Speaker
Port F---> HP2

AUD_PC_BEEP
AUD_CAP2
AUD_VREFFLT
C760 SC10U10V5KX-2GP
C761 SC10U10V5KX-2GP
PC BEEP
C780 SCD1U10V2KX-4GP
AUD_BEEP
R302 20KR2J-L2-GP
R587 10KR2J-3-GP
SB:70302
AUD_SYS_BEEP

+VDDA
U33 74AHC1G86GW-GP
From SB
ICH_SPKR 22
BEEP 32
From EC
XOR gate

+VDDA
R569 5K1R2F-2-GP
R573 39K2R2F-L-GP
C778 SC1KP50V2KX-1GP
HP1_NB_SENSE
Q64 2N7002-7F-GP
AUD_HP1_NB_SENSE 31,33
+VDDA
R300 5K1R2F-2-GP
R316 39K2R2F-L-GP
SB:70106
R313 20KR2J-L2-GP
C758 SC1KP50V2KX-1GP
AUD_HP2_NB_SENSE 22,31,33
MIC_SWITCH
Q24 2N7002DW-7F-GP
HP2_NB_SENSE
AUD_MIC_SWITCH

Change R352 to 2.67K
1% for AD1984

If SENSE_A total length
> 6" change C to 0.1uF

Azalia I/F EMI
ICH_AZ_CODEC_SDOUT
R578 47R2J-2-GP DY
ICH_AZ_CODEC_SDOUT1
C787 SCD1U10V2KX-4GP DY

Azalia I/F EMI
ICH_AZ_CODEC_BITCLK
R579 47R2J-2-GP DY
ICH_AZ_CODEC_BITCLK1
C788 SCD1U10V2KX-4GP DY

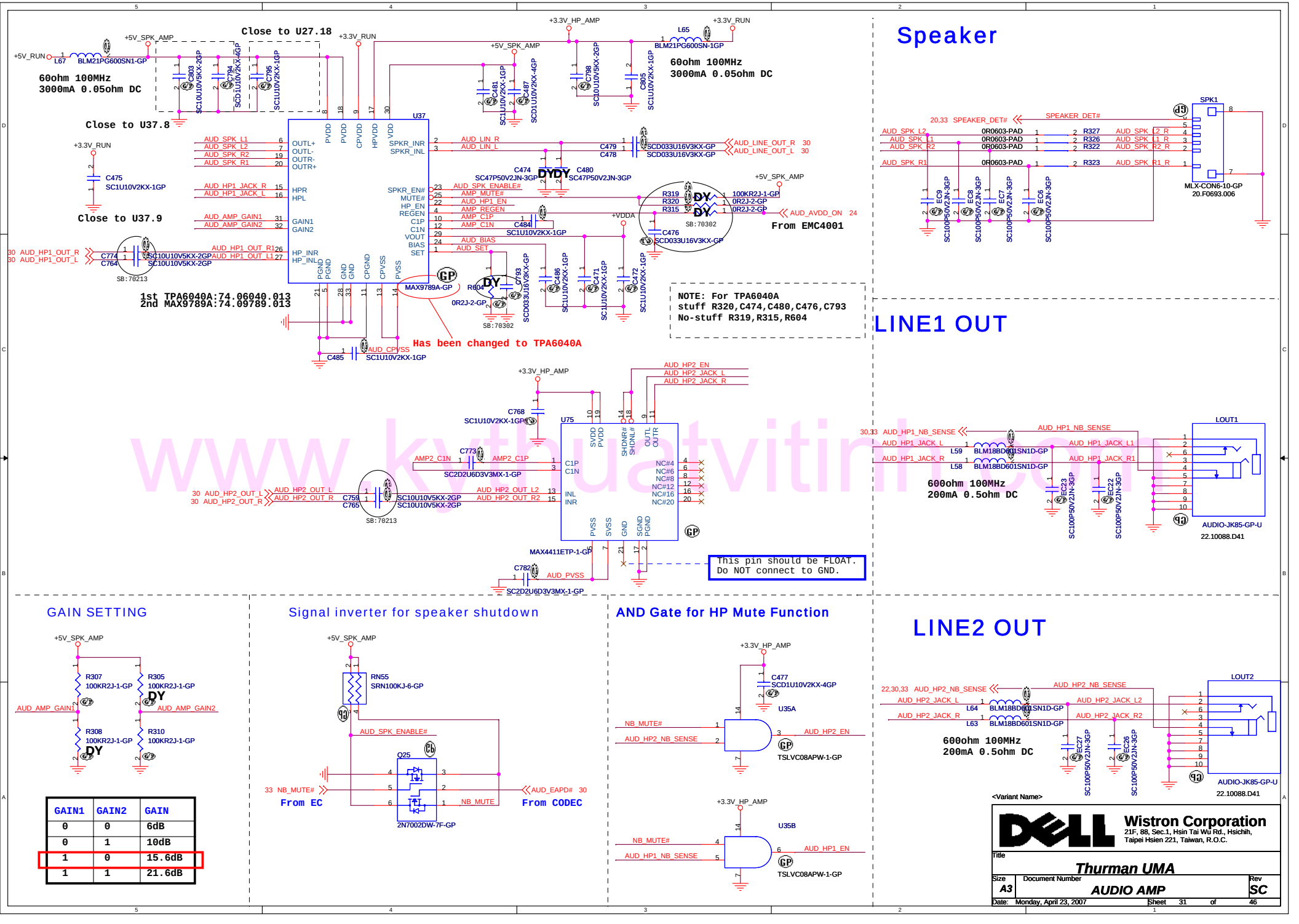
MIC IN
+3.3V_RUN
R602 100KR2J-1-GP
AUD_VREFOUT_B
R576 4K7R2J-2-GP
R599 4K7R2J-2-GP
C790 SC10U10V5KX-2GP
AUD_MIC_SWITCH
AUD_EXT_MIC_L
AUD_EXT_MIC_R
C785 SC1U10V2KX-1GP
C789 SC1U10V2KX-1GP
MIC_IN_L_2
MIC_IN_R_2
R586
R594
MIC_IN_L_3
MIC_IN_R_3
0R0402-PAD
BLM18BD601SN1D-GP L62
BLM18BD601SN1D-GP L61
MIC_IN_L_C
MIC_IN_R_C
EC25 SC100P50V2JN-3GP
EC24 SC100P50V2JN-3GP
MIC1
AUDIO-JK85-GP-U
22.10088.D41

600ohm 100MHz
200mA 0.5ohm DC

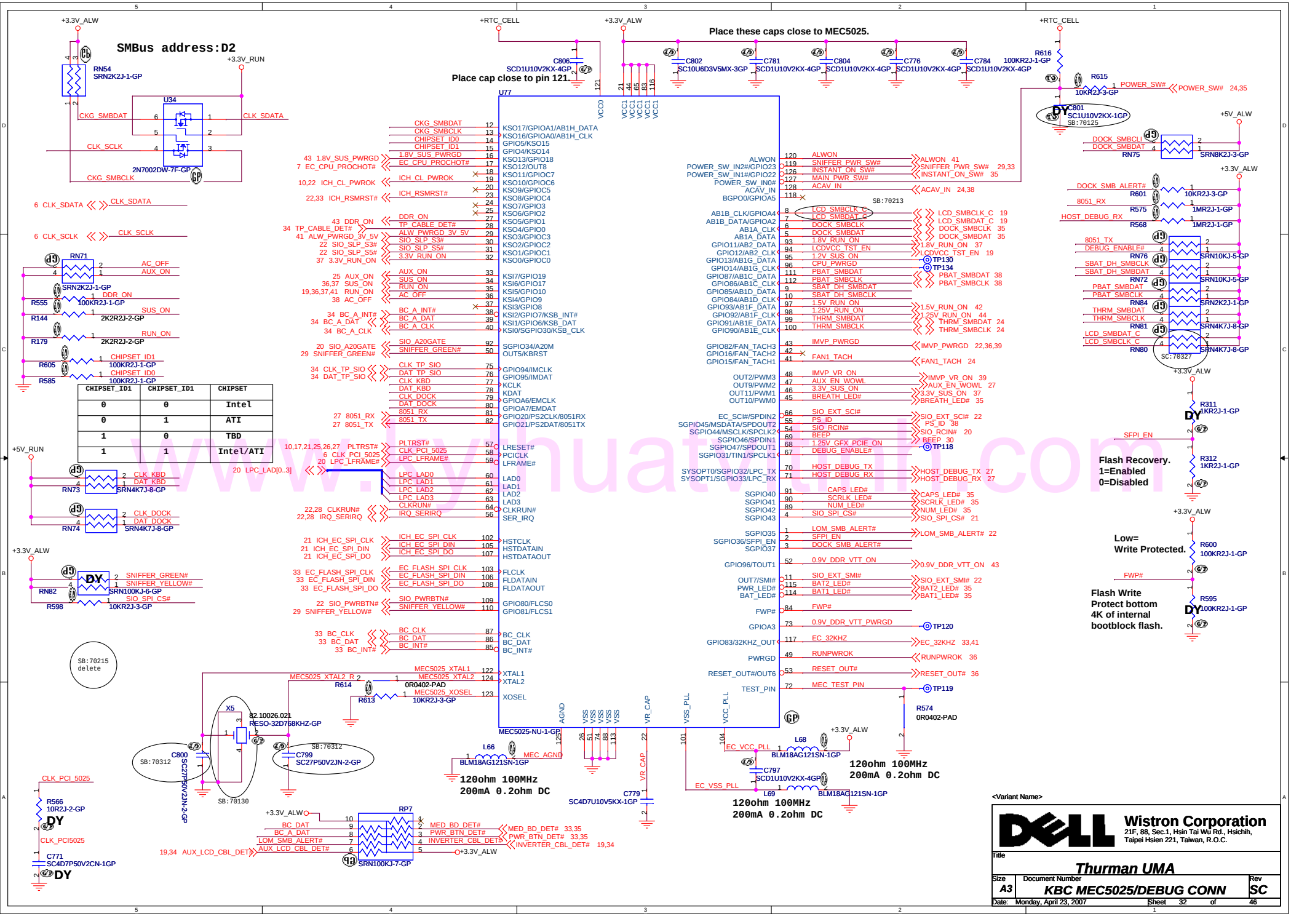
<Variant Name>

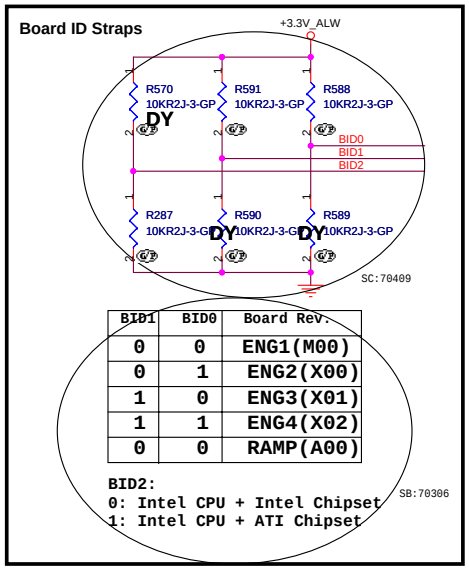
DELL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

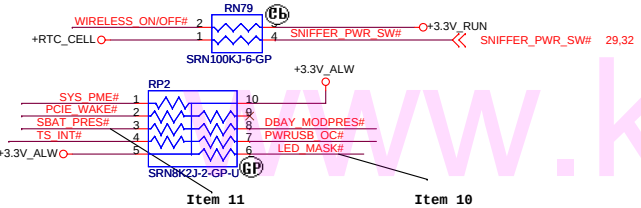
Title: Thurman UMA
Size: A3
Document Number: CODEC STAC9228
Rev: SC
Date: Monday, April 23, 2007
Sheet 30 of 46

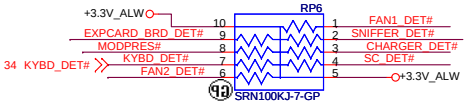


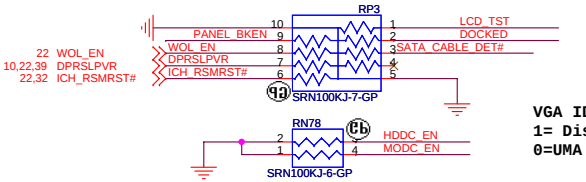
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

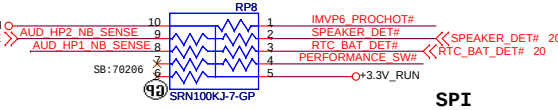


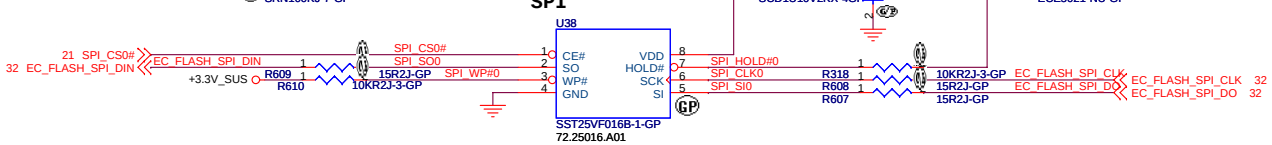


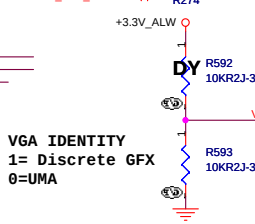


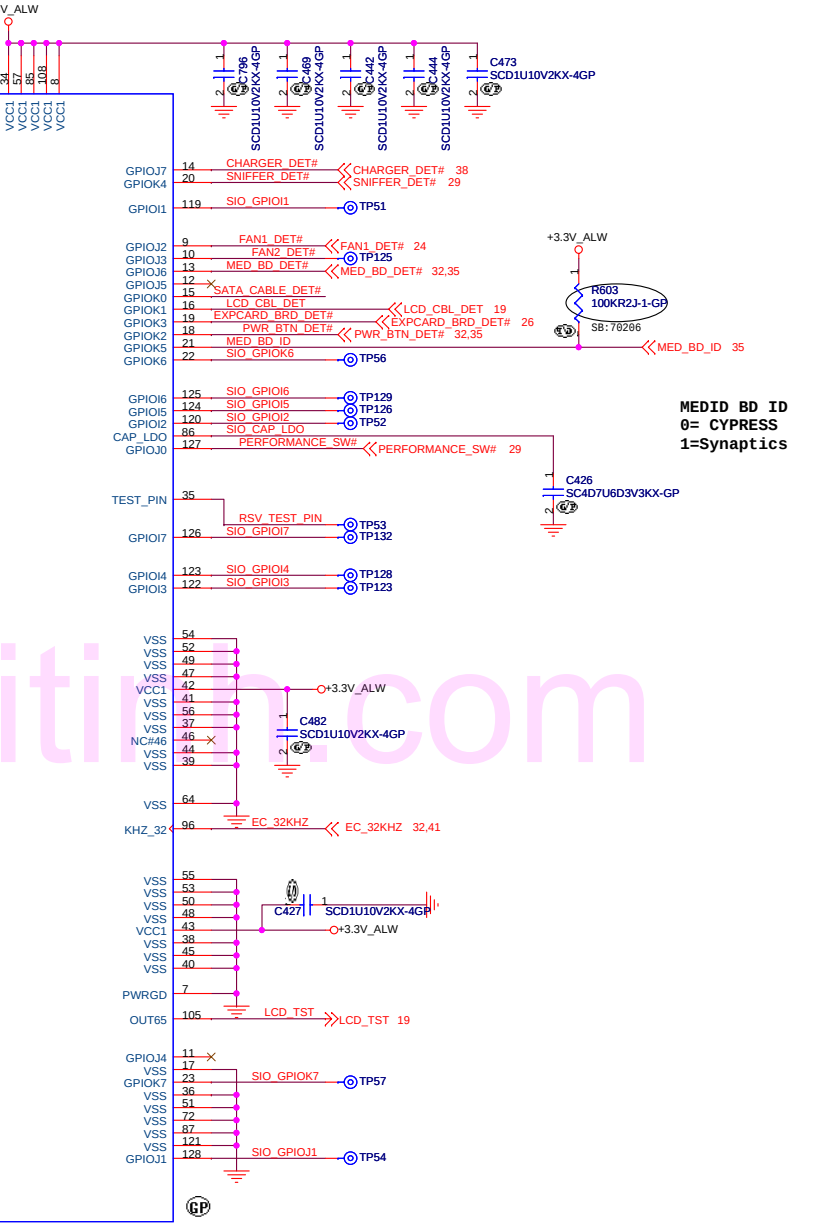












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Title: Thurman UMA

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A3	SIO ECE5011/SPI ROM	SC

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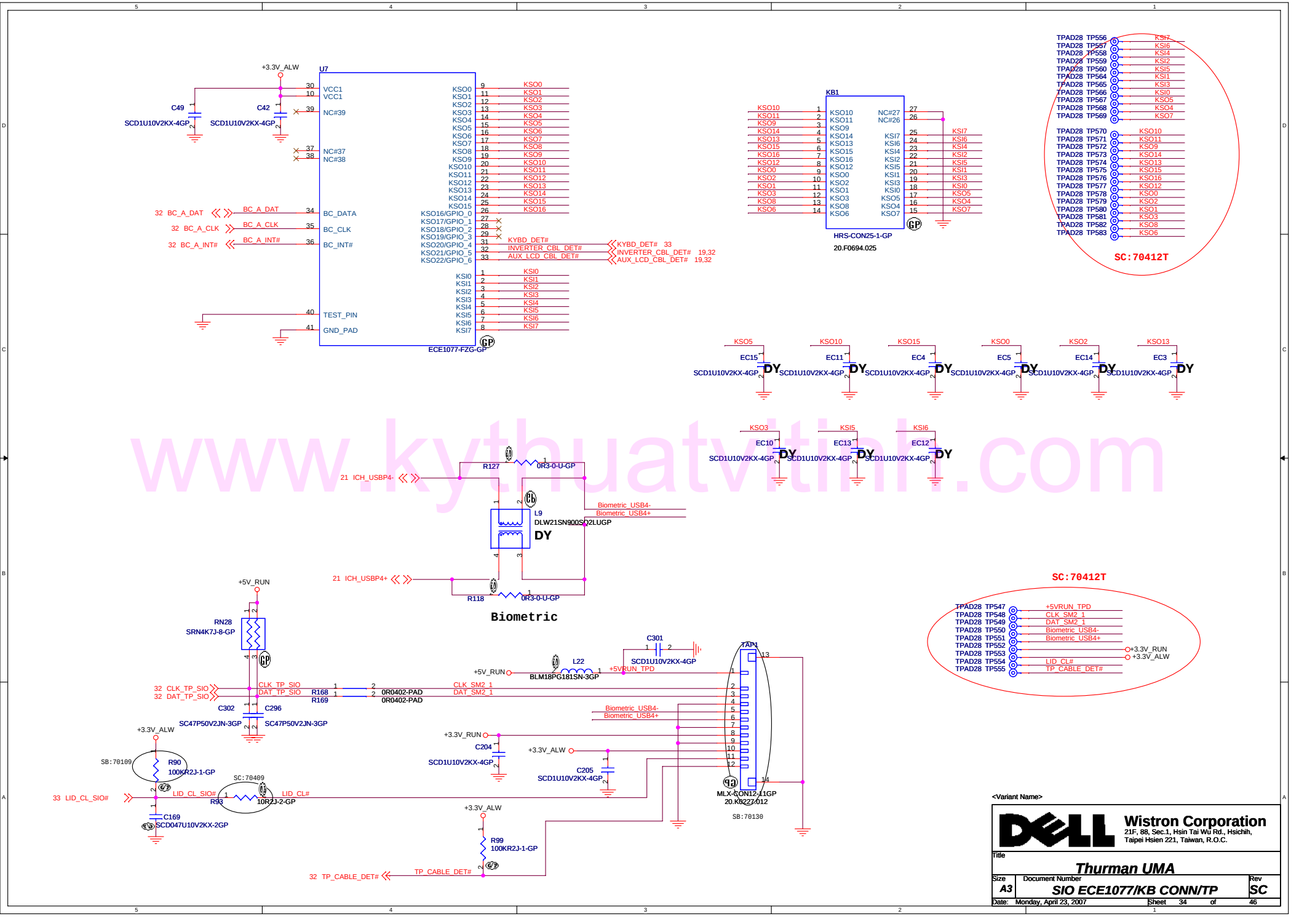

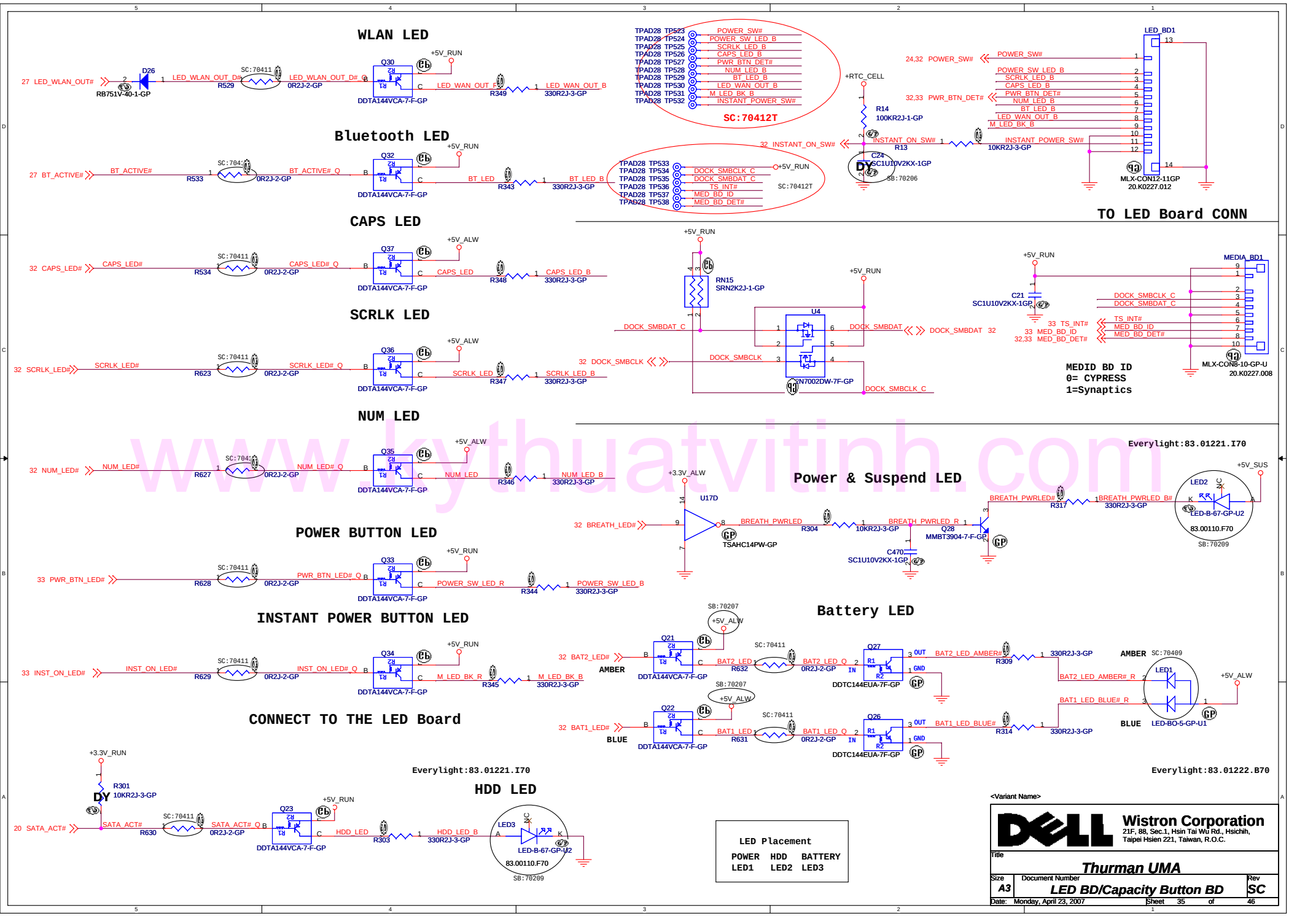

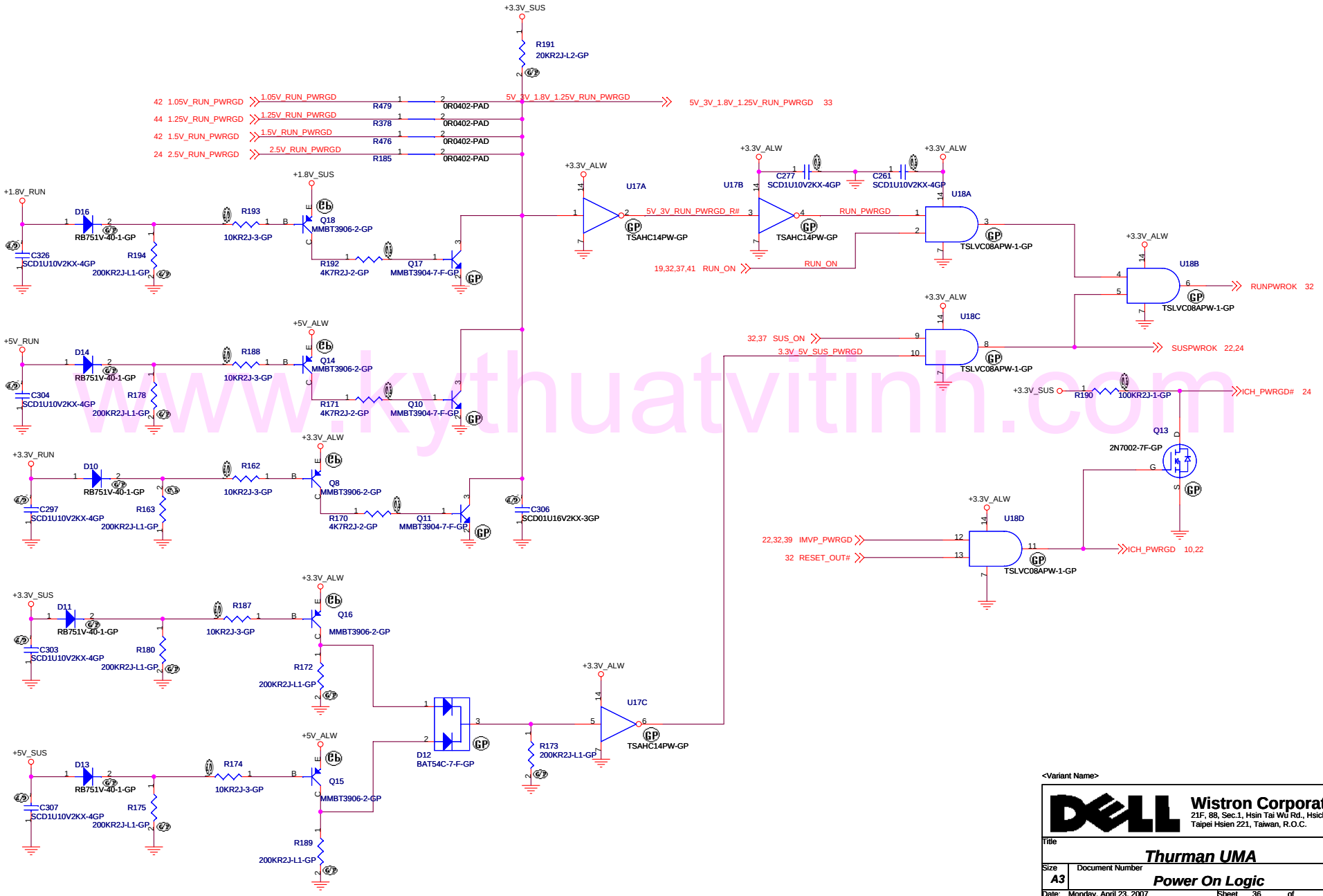

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Title: Thurman UMA

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A3	Power On Logic	SC

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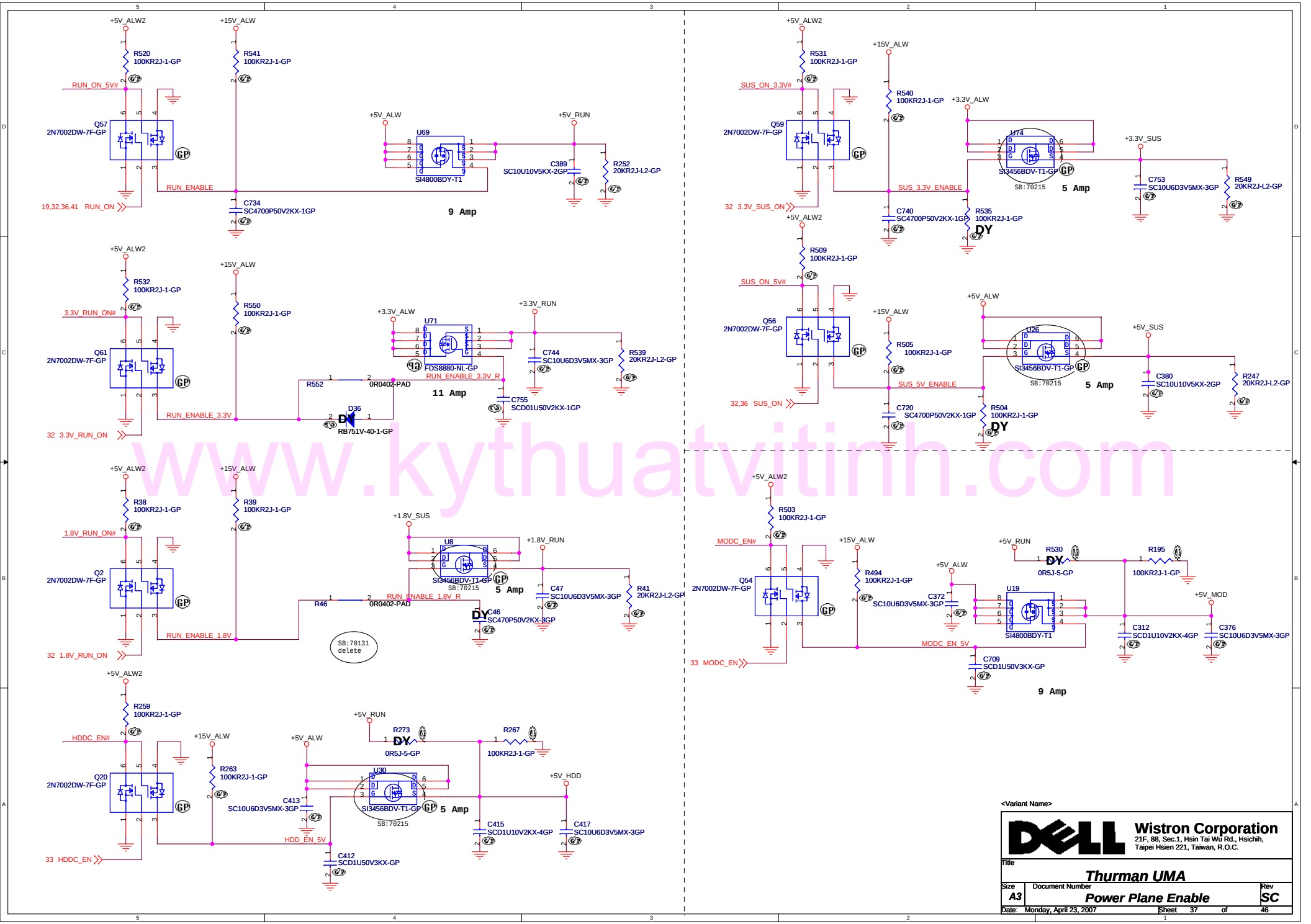

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Title: Thurman UMA

Size: A3 | Document Number: Power Plane Enable | Rev: SC

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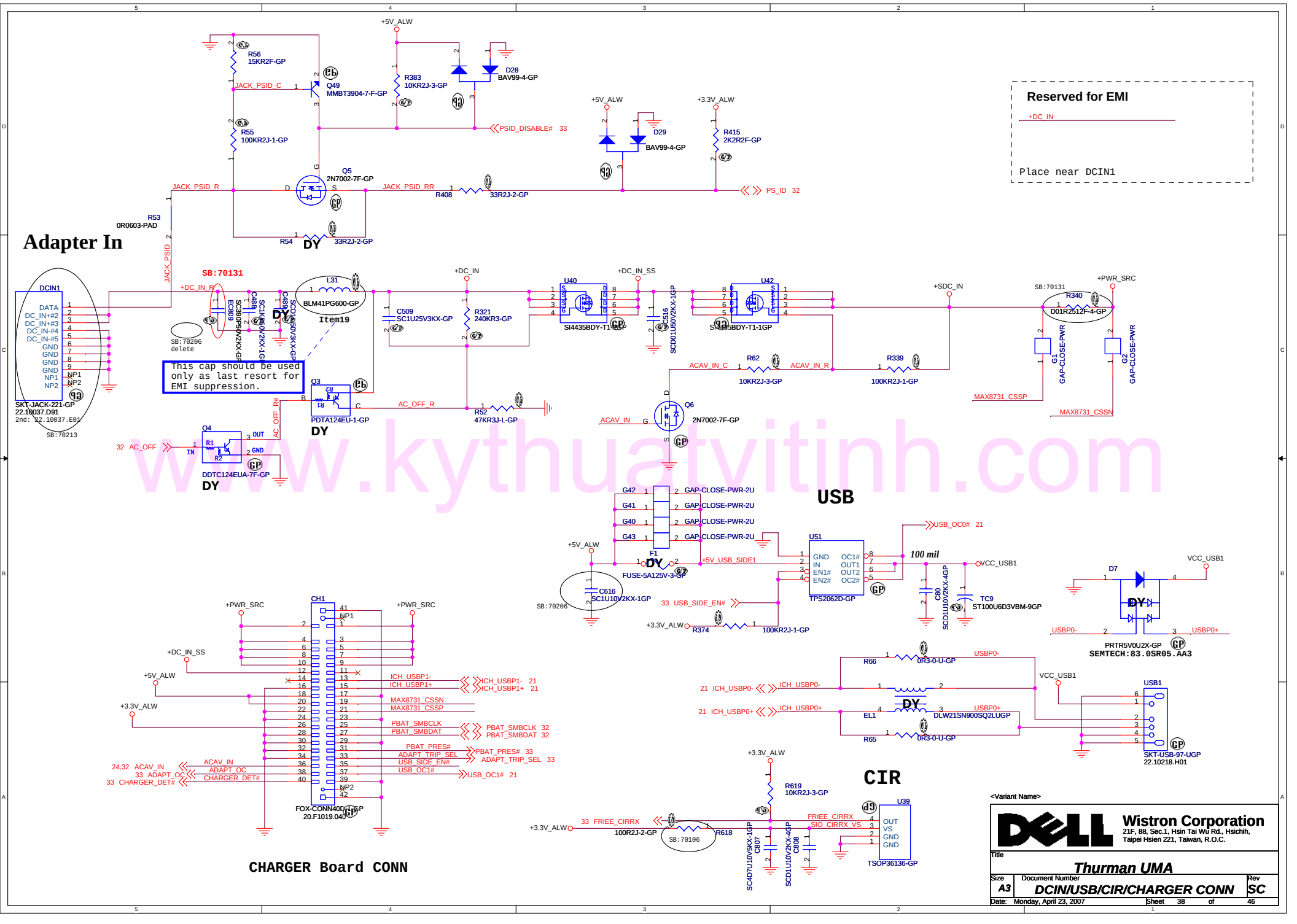
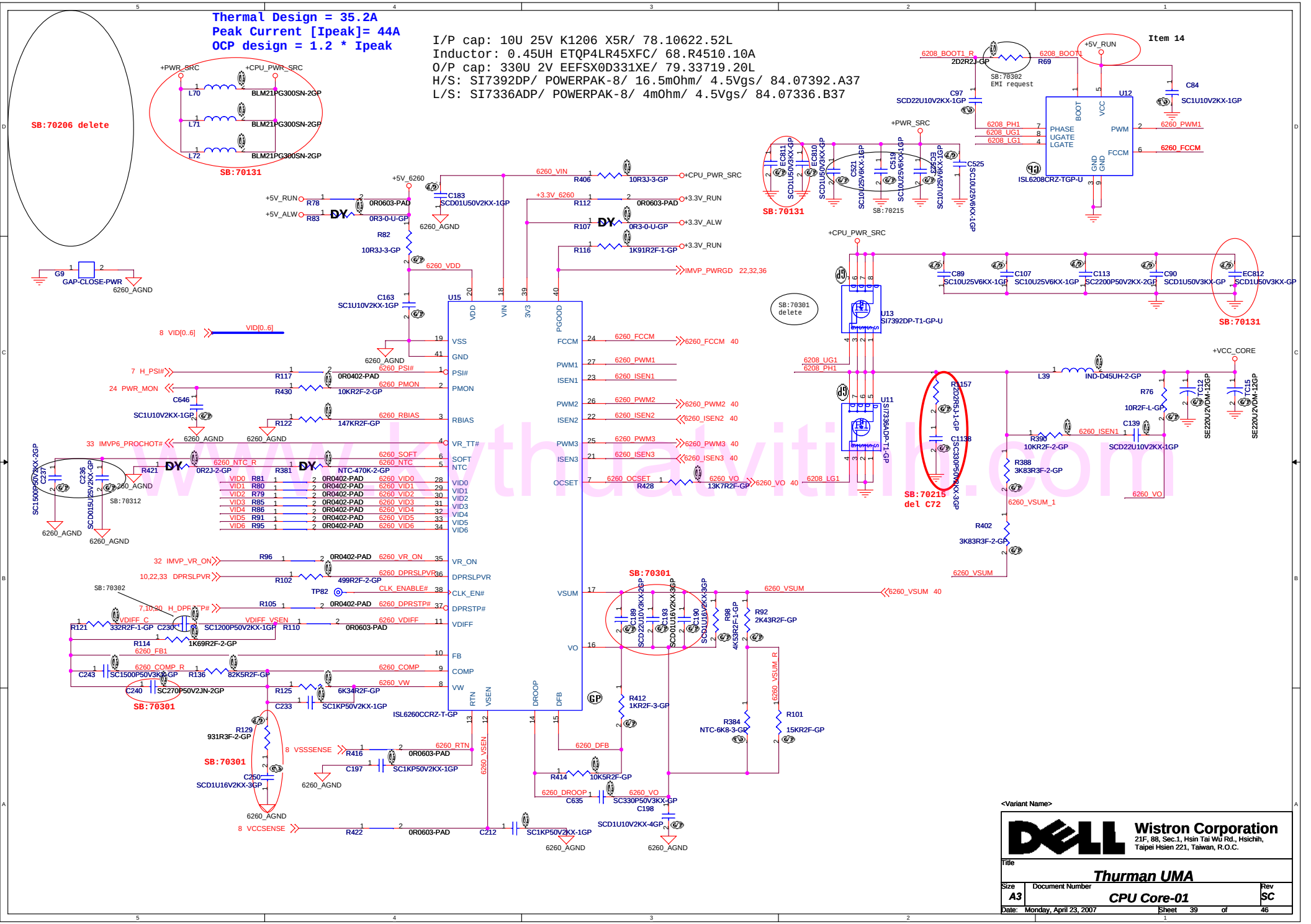


Thermal Design = 35.2A
Peak Current [Ipeak]= 44A
OCP design = 1.2 * Ipeak

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A
O/P cap: 330U 2V EEFSX0D331XE/ 79.33719.20L
H/S: SI7392DP/ POWERPAK-8/ 16.5mOhm/ 4.5Vgs/ 84.07392.A37
L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37

SB:70206 delete

Item 14



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Title: Thurman UMA

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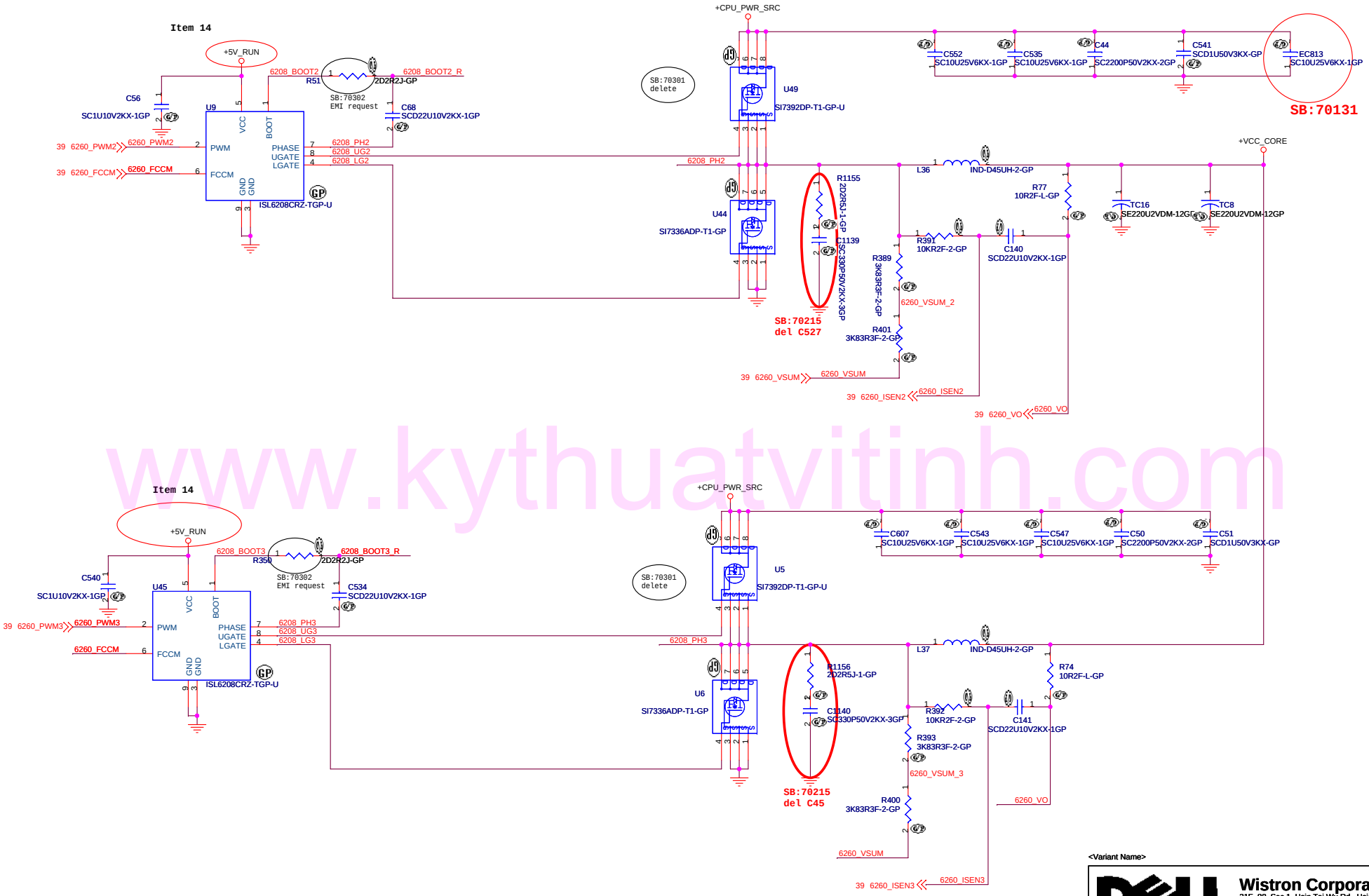
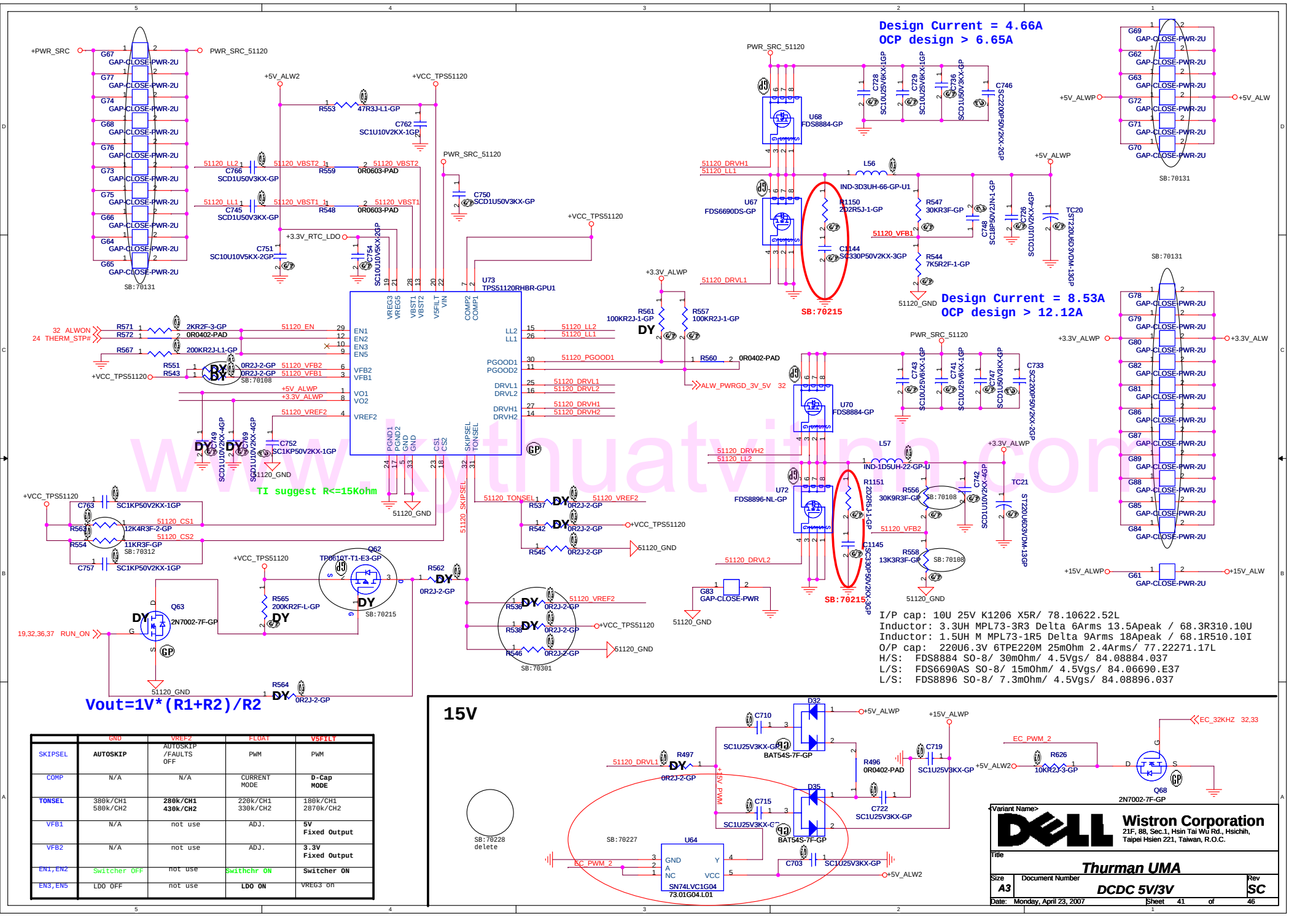
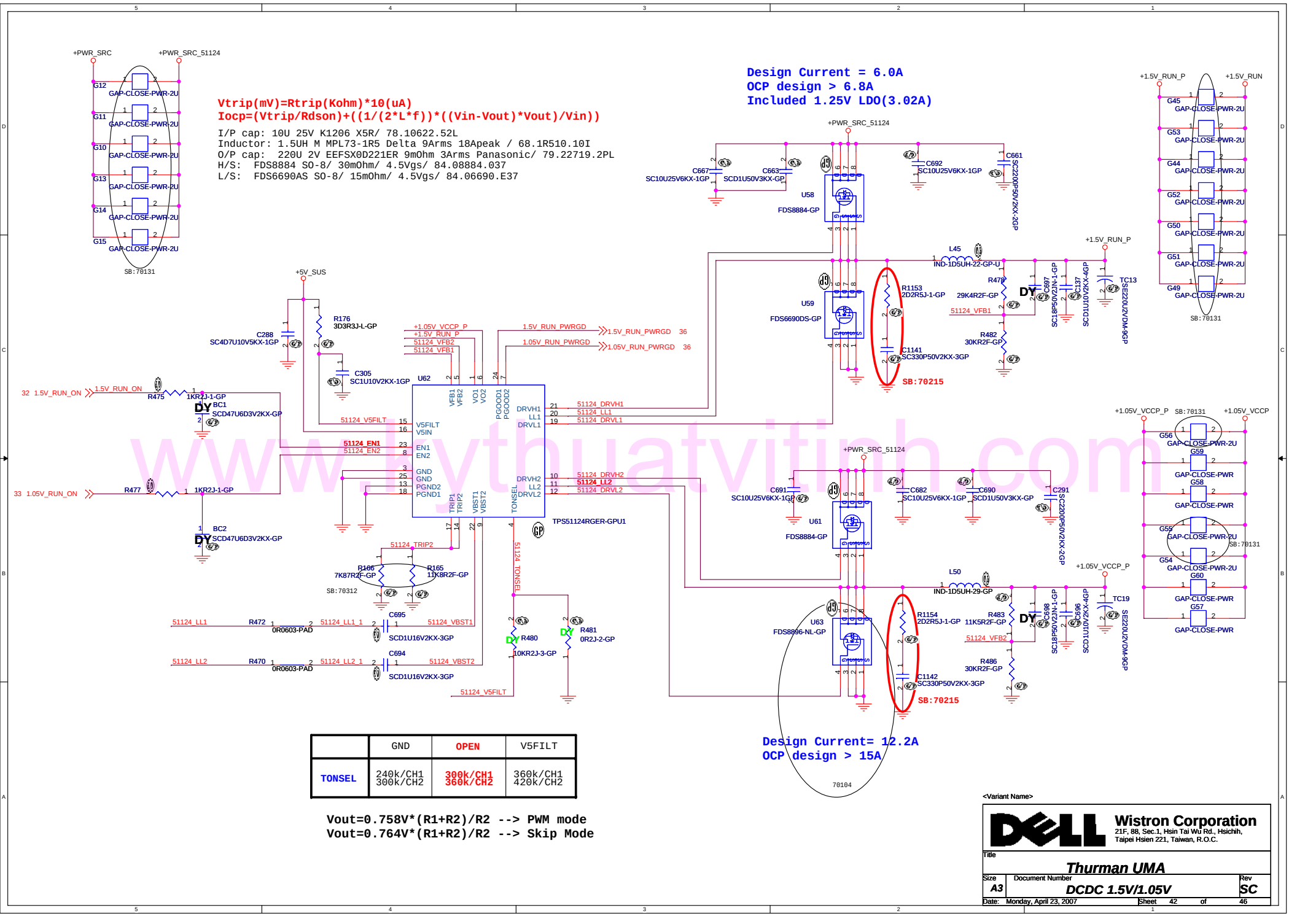
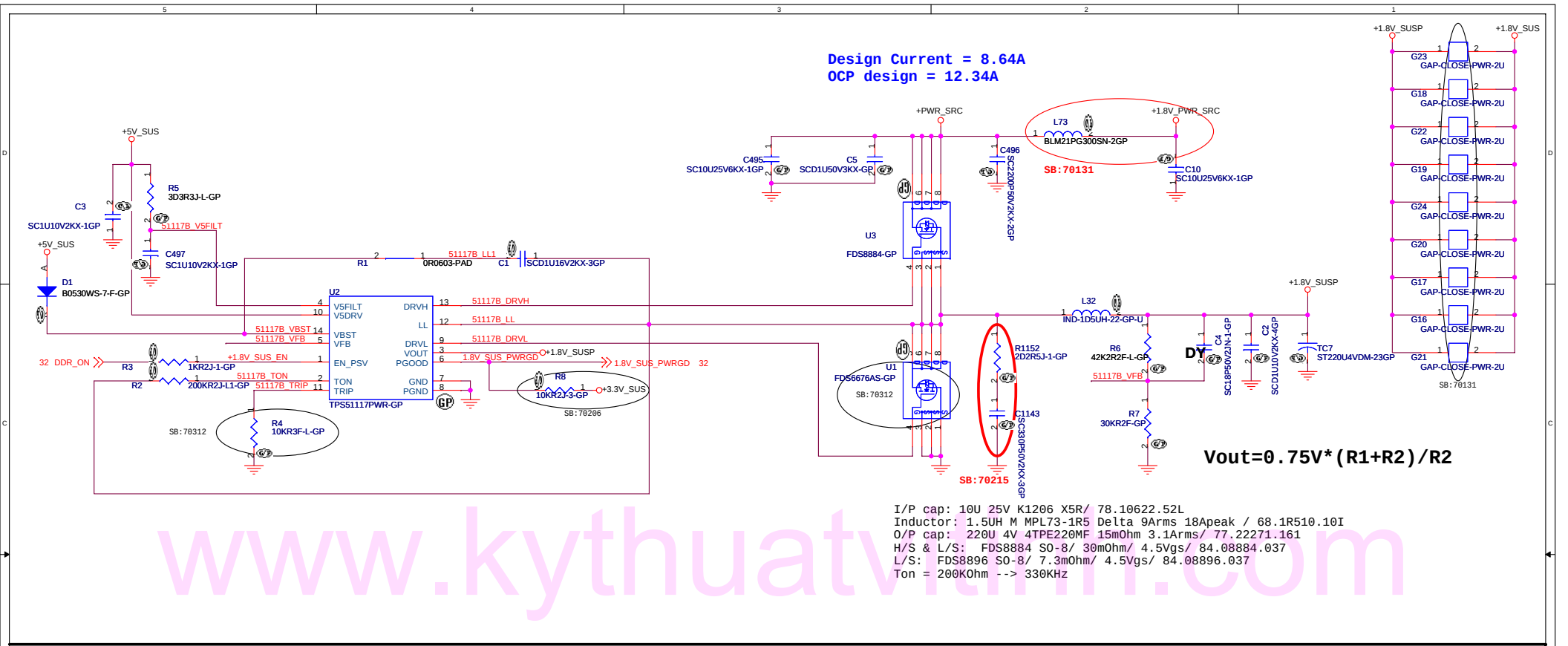




	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	**280k/CH1 430k/CH2**	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2



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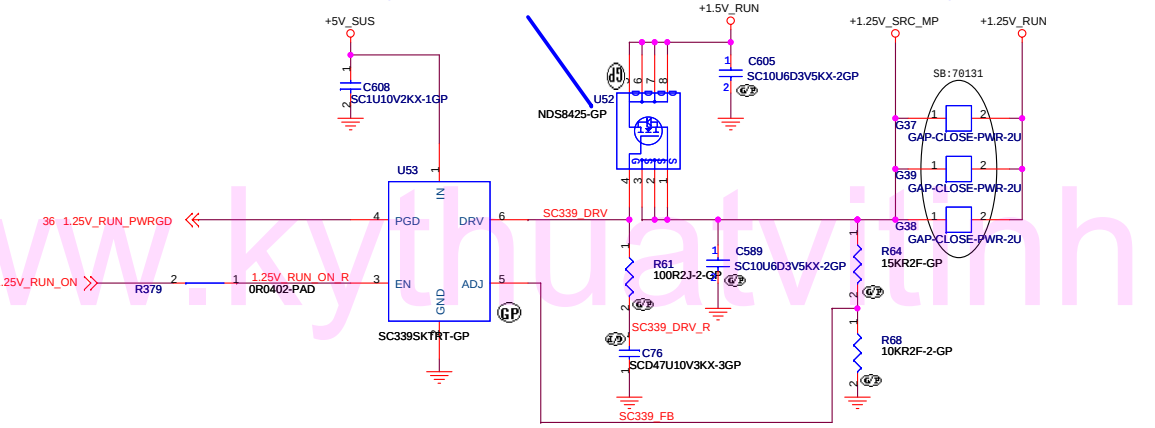
Will Change to NDS8425. 28mOhm/@2.7V **Design Current = 3.0A**



<Variant Name>

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Title	Thurman UMA	
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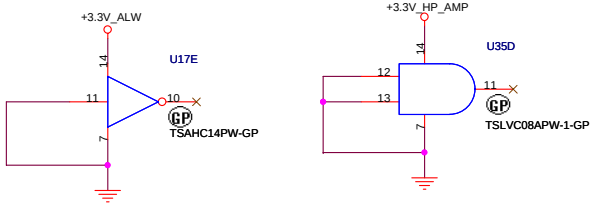
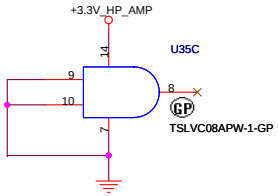
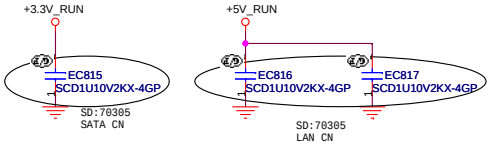
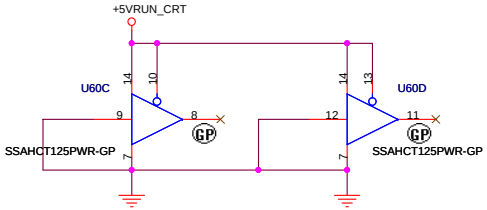
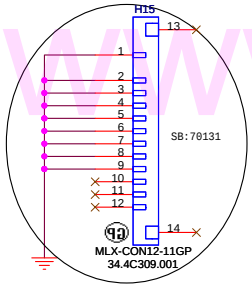


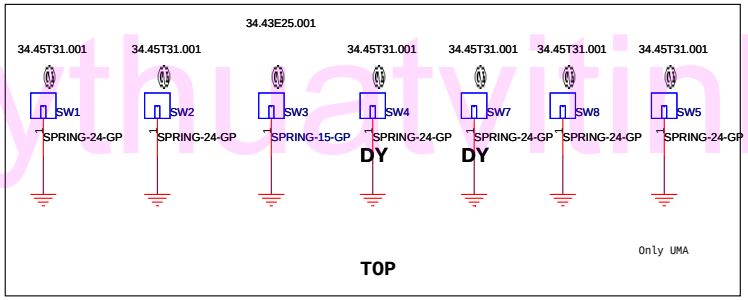


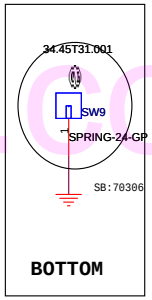


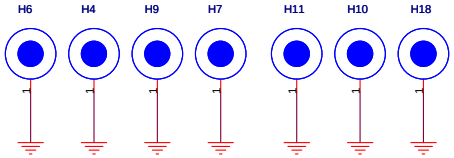


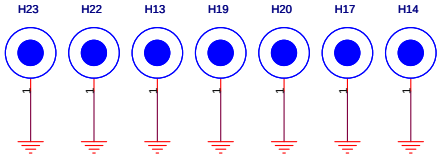
SW3 - 34.43E25.001
SW9 - 34.49Q02.001
SW5 - 34.34T31.001 (Only for UMA)
others-34.45T31.001











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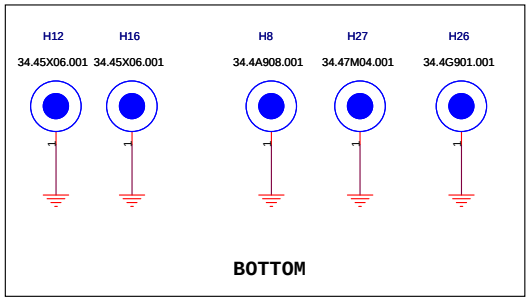
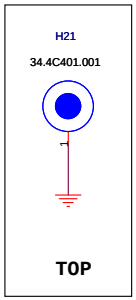
H21: 34.4C401.001





<Variant Name>

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Title: Thurman UMA

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		11				EE
		12				EE
		13				EE
		14				EE
2006/11/24		15				EE
		16				Power team
		17				EE
		18				EE
		19				EE
		20				EE
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